DESIGN AND FABRICATION OF MULTI-CHANNEL SCALER

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In Partial Fulfilment of the Requirements
for the Degree of
MASTER OF TECHNOLOGY

By
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CERTIFICATE

This is to certify that this work on "THE DESIGN AND FABRICATION OF THE MULTI-CHANNEL SCALER" has been carried out under my supervision and has not been submitted elsewhere for a degree.

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ABSTRACT

A Multi-channel Scaler (MCS) has been designed to eliminate the need of an expensive Multi-channel Analyzer in the everyday use of a Mossbauer Spectrometer. With suitable changes in the hardware, this unit can also be used for Computer Averaging of Transients, as necessary for NMR spectroscopy and so on.

The instrument is designed to be compatible with a programmed-velocity Mossbauer Spectrometer having 256 different values of velocity (referred to as "Channels") repeated per signal cycle. Thus the total number of locations provided in the main memory of the instrument has been chosen to be 256, each location having a maximum data capacity of 6 digits. Provision has been made to expand the number of channels further, if desired.

Special arrangements have been made to seek independence, whenever desired, from the Mossbauer Spectrometer, once an experiment is over and data is stored in the memory. For this purpose two modes - CLOCK and FREE - have been provided in the instrument. During the CLOCK mode the data pulses are accepted and the instrument obeys the commands coming from the Spectrometer. During

the FREE mode these commands are ignored and no data is accepted. Display is possible in either mode.

Provisions have been made for a CRO X - Y display of Channel Count versus Channel Number. A Nixie display that simultaneously displays the Channel Number and the Channel Count has also been incorporated. The instrument also generates commands for a type writer to facilitate a hard copy of the experimental results.

Provisions have been made for the protection of the data, accumulated in the instrument, against a power failure. For this purpose key units are supplied with back up power from DC batteries. The instrument is automatically switched on to FREE mode, the instant power fails and the incoming data as well as the command signals from the Spectrometer are ignored.

CHAPTER I

INTRODUCTION

1.1 The Principle of Multi-channel Scaling (MCS)

The basic principle of operation of the Multi-channel Scaler is signal accumulation. A number of cycles of a repetitive signal are synchronously accumulated in a memory. The different locations in the memory are referred to as "Channels", which are explained in detail in Section 1.2. The accumulated signal is a scaled version of the original and hence the name Scaler.

The technique of multi-channel scaling plays a very important role today in many fields of experimental research. Its obvious use is in the experimental study of statistical phenomena, where an experiment is repeated under exactly identical conditions for a large number of times and the data, which is governed by probability laws, is accumulated in the memory. The MCS is also used for the purpose of Signal Enhancement. The synchronous addition of different cycles of the same signal results in the cancellation of random noise, and the signal to noise ratio is enhanced.

Today, the MCS finds its main use in the Mössbauer Spectroscopy. It is also invariably used in the fields

of Nuclear Magnetic Resonance (NMR) and alike, where it is referred to as Computer Averaged Transients technique (CAT).

The present model of the MCS is to be put to an immediate use in Mossbauer Spectroscopy and hence it is designed to suit the specifications determined by a general Mossbauer Spectrometer.

1.2 The Channels

For the purpose of synchronous addition it is obvious that the signal cycle has to be divided in to an appropriate number of segments. Each of these segments is referred to as a "channel". A separate location in the memory is assigned to each channel, and the signal is cumulatively stored in different memory locations corresponding to different channels. The process of addition would need an adder which should access the particular memory location, add the current value of the signal to the accumulated value stored for that channel and store the result of the addition back in the same location as shown in Fig. 1.1.

1.3 Input Output Facility

The memory required and the process of addition advocates the usage of binary system in the instrument.

It also demands the current value of the signal be processed and made available to the adder in the binary form, through a proper interface. In Mossbauer Spectroscopy the data is in the form of pulses, so we need a counter at the input. In case of NMR the data is an analog signal and hence the interface is an A/D converter. Since the instrument is specifically designed for the Mossbauer Spectroscopy, we shall hence-forth refer to the contents of the memory locations as the corresponding 'channel counts'.

The system should have a capability of plotting the channel count versus channel number, to obtain the complete picture of stored signal. This is very important for checking whether the experiment is running on proper lines or not. We therefore have made a provision for X-Y display using a CRO.

For the detailed analysis of the experiment, the user would be interested in the count of a particular channel. Hence the display unit should have a programmable access to the memory, and should have provisions for simultaneously displaying the channel no and its count, preferably in decimals, for easy interpretation. We have made provisions for Nixie tube display.

For the hard copy of the experiments the instrument also has a provision for type writer output.

1.4 Relevant Feature of Mossbauer Spectroscopy

As the data is to arrive from the Mossbauer Spectrometer, a brief attempt is made here to project relevant features of the Mossbauer Spectrometer which will determine the specifications of the MCS. (Fig. 1.2).

The crystal oscillator generates a rectangular wave of high frequency stability the scaler scales down the frequency to appropriate value suitable for driving the mechanical movement used in the Drive System. The radio active source mounted on this movement emits γrays which reach the Detector, through an absorber, consisting of the material under investigation. The output pulses generated by the Detector are sent to the Single Channel Analyzer that selects the γ rays that have energies withing a specified band and sends them to the MCS.

The purpose of the experiment is to study the distribution of these unabsorbed γrays against velocity of the source. MCS start pulse defines the zero crossing of this velocity. The channel clock is used to synchronise the input data to the MCS with the channel numbers.

The +ve half of the channel clock defines the channel window. The window that starts just after the positiv edge of the MCS start pulse defines the 1st channel.

The mechanical movement defines the frequencies of various signals in the Mossbauer spectrometer. This is generally 10 - 100 Hz. The number of channels determines the capability of resolution. Most systems have 256 or 512 channels. Obviously the channel clock then falls within the range of 2.5 KHz to 50 KHz.

The Mossbauer spectrometer in the Nuclear Physics Department of I.I.T./K. has a 20 Hz motion and a clock of 5/10 KHz specifying 256/512 channels.

1.5 Independence of the MCS

Once the signal is accumulated in the MCS and only the channel counts are to be read, the user should be able to switch off the Spectrometer and the SCA. from the system. In such an event the MCS would not be getting the channel clock and the MCS start, and should be in a position to preserve and display the accumulated data without them. We have made such a provision in the MCS, in the form of CLOCK and FREE modes. In the Free mode the MCS neglects the MCS start and the channel clock, and

the incoming data is not admitted. The data is preserved and all the 3 forms of displays are possible.

1.6 Power Failure Safeguard

A typical Mossbauer Spectroscopy experiment runs for tens of hours, and hence special precaution has to be taken to preserve the accumulated data and restart the experiment once power comes back. No data should be admitted once the power fails. In the present unit the data is preserved, and a fresh intake of the data can be had after power comes back by switching on to Clock mode.

1.7 Specifications

Channel number 256 (expandable to 512 and higher if necessary)

Channel Clock 2.5 KHz - 50 KHz

Channel count 999999 maximum

Nixie display

C.R.O. X - Y display

Typewriter Output Facility

Independence from Spectrometer when desired

Power Failure Safeguard.

1.8 Introduction to Chapters

The thesis has been divided in 6 Chapters. The second chapter presents the System Design. It also explains the choice of components used and arrives at various signal commands required.

The various Units employed are described in Chapters 3,4.and 5. Chapter 3 deals with the Control Logic and the Arithmetic Unit. Chapter 4 describes the Display Unit while the Power Failure Safeguard is discussed in Chapter 5. Chapter 6 offers the suggestions for improving the System Performance.

CHAPTER II

SYSTEM DESIGN

The chapter deals with the various system requirements to meet the set ofspecifications given in Section 1.7. It also explains the choice of various components used and arrives at the various signal commands required to facilitate the operation. Section 2.1 describes the primary building blocks. The data structure and the choice of memory is dealt with in Section 2.2 and 2.3 respectively. Section 2.4 through Section 2. develop the detailed block diagram of the system.

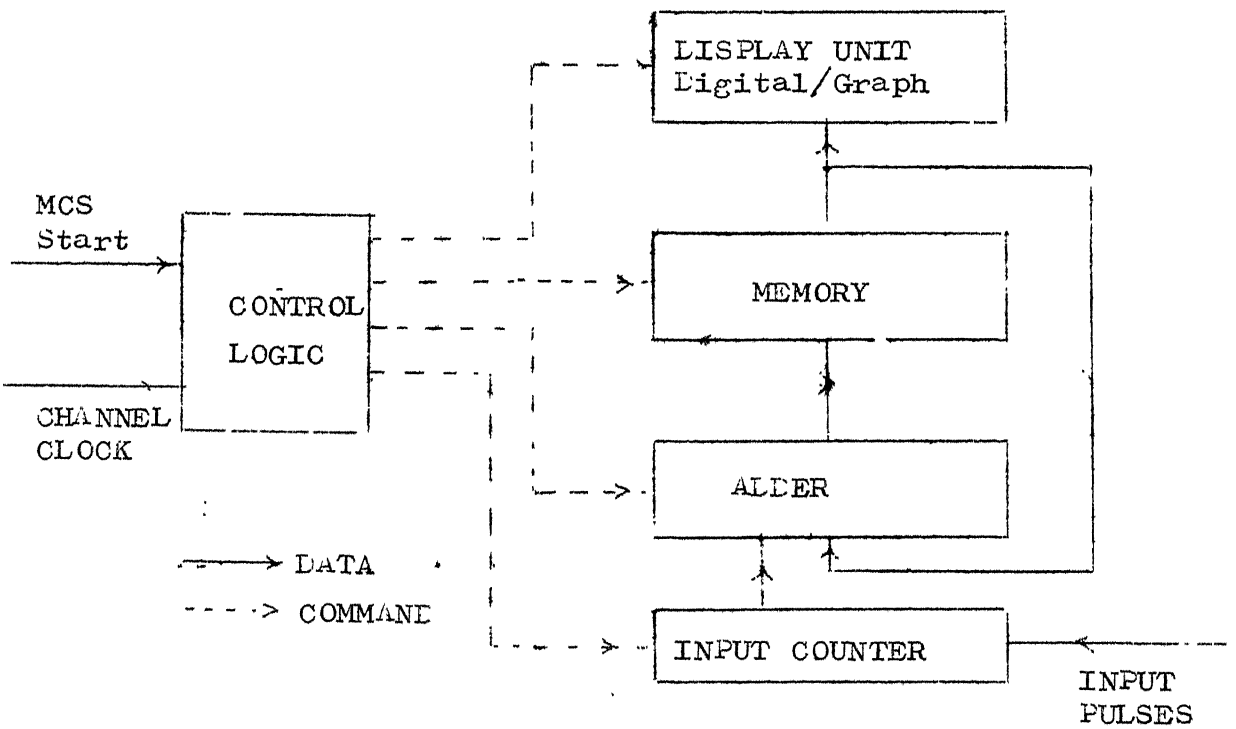


Fig. 2.1 THE BUILDING BLOCKS

2.1 The Building Blocks

Figure 2.1 presents an elementary block diagram of the system. As the instrument is required to aggregate the number of pulses corresponding to each of the individual channel over a period of time we need a memory, preceeded by an arithmetic unit and a counter to count the input pulses, that arrive during the channel window. The display unit should have a programmable access to the memory output. A Control Logic will have to be designed for appropriate command of the operations of these 4 blocks. The main functions of this Control Logic would be

1. To tag the memory locations with their channel numbers for proper identification;
2. To provide programmable access to any chosen memory location;
3. To open the input counter during a channel window;
4. To add the output of the input counter at the end of the channel window to the accumulated contents stored in the memory location corresponding to that channel;
5. To store the result of step 4 back in the memory location corresponding to the same channel;

6. To clear the input counter once step 5 is over;

7. To ensure that the input to the 1st channel is enabled just after the MCS start pulse;

8. To provide arrangements for erasing the memory completely before the start of an experiment;

9. To ignore the MCS start and the channel clock when switched to FREE mode as explained in Section 1.5;

10. To provide power failure safeguards.

2.2 Code and Structure of Data

The most important factor in any numeral binary system is the code followed. As the only arithmetic operation to be performed is that of addition, the choice is obviously between Binary and BCD. In our system each channel has a six digit capacity. A choice of binary code would save the number of bits required (20 against 24 required for BCD). But as the display has to be decimal and as the hardware required to convert, a 6 digit binary to BCD for display offsets this saving of bits, we prefer the BCD code.

The next design consideration is the mode of access to the memory. The access to the channels will always be serial to match their occurrence in real time. As the

system is quite slow - maximum channel clock frequency 25 KHz - there is no advantage of providing a parallel access to all the bits of a channel. On the other hand having only a bit wise serial access will involve a change in the nature of the mathematical operation after every four bits. The optimum saving of hardware is therefore obtained if we have parallel access to all the four bits belonging to the same digit while access to the digits remain serial. This renders the addition operation exactly repetitive, particularly in view of the fact that the count is always between 0 and 9 in the input counter.

2.3 Choice of Memory

The factors to be considered before arriving at a particular choice of memory are the size of the memory required, the speed requirements, the cost analysis and the particular advantages and disadvantages of the memory type.

The size:- For 256 channels, each having a capacity to store a 6 digit BCD data the size required is $256 \times 6 \times 4 = 6144$ bits.

The speed:- Channel clock frequency - Minimum 2.5 KHz, Maximum 50 KHz.

Memory access rate - Minimum 15 KHz, Maximum 300 KHz.

The available memory types in this frequency range are

1. Bipolar
2. Magnetic
3. MOS memories.

We first discuss the attributes of these memories and arrive at a particular memory type.

The Bipolar memory is basically a high speed memory far exceeding the speed limitations of both MOS and Magnetic. Its high frequency limitations are in MHz where as there are no low frequency limitations. Moreover, its signal levels are the same as the rest of the logic. But one of its very serious drawbacks is the power consumption which typically ranges between 1 - 2 mw/bit. For our size the memory alone would consume 6 - 12 watts. This is quite a large amount to be dissipated. Another factor is the volatality. The data is lost in case of a power failure which means, if at all we use back-up arrangements we have to supply so much power to the memory alone.

The magnetic memory has the inherent advantage of non-volatality. It also offers access time under 1 micro-

second. But they operate at signal levels much higher than the peripheral logic which needs quite elaborate and costly system of sense amplifiers and drivers. Moreover the readout is destructive and hence the cycle time is 2 - 3 times the access time. As our high frequency limitations are not very critical, this factor is not of much consenquence to us. But the cost requirements of drivers and sense amplifiers are rather prohibitive.

The third possibility is the MOS memory. This is a volatile memory and requires back up power if we want to preserve data during power failure. It is slower as compared to Bipolar, but is slightly faster than its magnetic counterpart. Its high frequency limits are in MHz. But the greatest advantage of this type of memory is the low power consumption typically less than .1 mw/bit. As a consequence it has got high density, leading to a reduction in chip count for large memories.

We have adopted a digit-wise serial access in channels which themselves in turn are accessed serially. From the discussion in Section 2.2, we can see that we basically need four 1536 bit serial access memory blocks with single input-output as shown in Fig. 2.2.

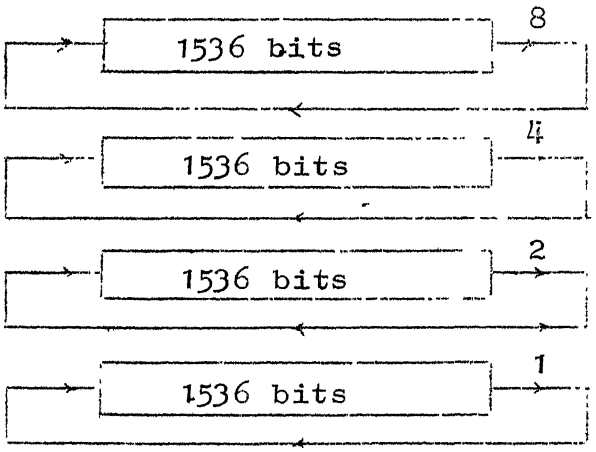
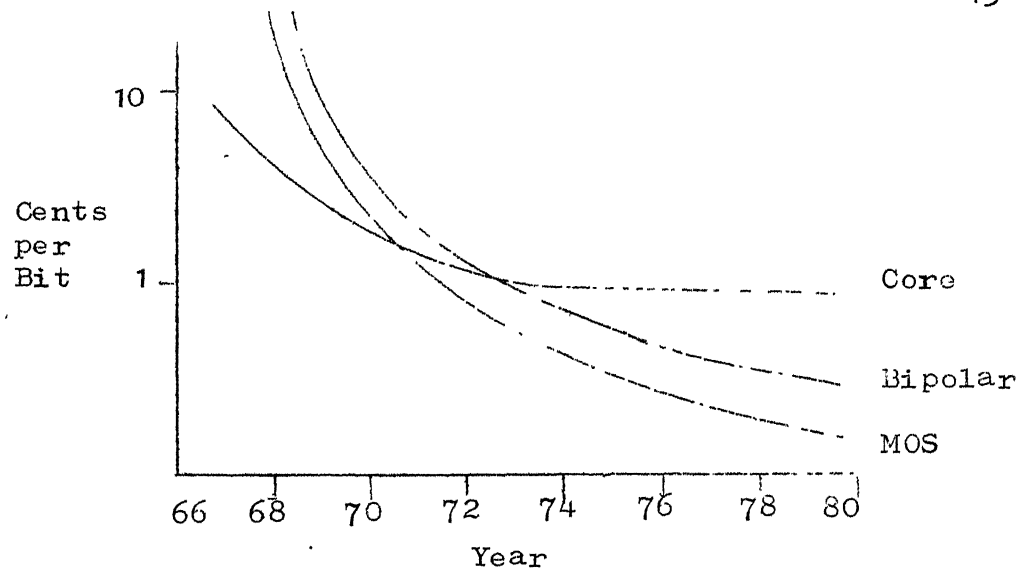


Fig. 2.2 THE MEMORY BLOCK ORGANISATION

This purpose is best served by MOS shift registers. Today MOS chips are available with as high as 2048 bits per chip and have potentials of offering much higher bit densities. The MOS shift registers thus have a distinct advantage over their Bipolar counterparts. The magnetic memory is basically random access and added hardware is required to achieve a serial access.

From the above discussion we find that the MOS shift registers have a distinct edge over the other two. Next we come to cost analysis, the most important factor, as the memory is the costliest component involved. We refer to the cost analysis curves, given by Mr. Robert F. Graham and Dr. Marcian E. Hoff, Intel Corporation in the Electronic Products, January 1970, reprinted in Intel Article reprint.



THE MEMORY COST CURVES

The previous discussion and the above curves project the MOS shift registers as the natural choice. Having decided about MOS shift registers we have to make a choice between static and dynamic. The choice is guided by the peripheral circuitry and hence is postponed till Section 2.6

2.4 The Control Logic

The function of Control Logic have already been explained in Section 2.1. In this section we deal with those function which have a bearing on the overall system design. The Control Logic has to provide the memory advance pulses. As 6 digits are stored serially in each channel the Control Logic in effect has to generate a burst

of 6 pulses that fall within the period of the Channel Clock supplied by the Mossbauer Spectrometer. The MOS shift registers in general would need 2 sets of such bursts, one for reading and one for writing. Hence we need two such clock burst generators (CBG) with appropriate phase relations. Both of these are to be controlled by the Channel Clock. To be able to identify which of the six digits corresponding to a channel is available at the memory output a 6-line decoder is attached to the counter used for the Read CBG. Line L_1 is high when the LSD appears and L_6 is high when the MSD appears.

The next function of the Control Logic is to control the Arithmetic Unit. To show how this is achieved we refer to the timing diagram of Fig. 2.3. For the sake of clarity we take a specific memory, TMS 3401 with 2 clocks C_1 and C_2. The output appears after the negative edge of C_2, and the data is loaded at the positive edge of C_1.

The write pulses are generated within the instrument whereas the Channel Clock comes from the Spectrometer. To put as few restrictions as possible on the Channel Clock we use a parallel mode buffer memory - a shift register with parallel loading - after the input counter.

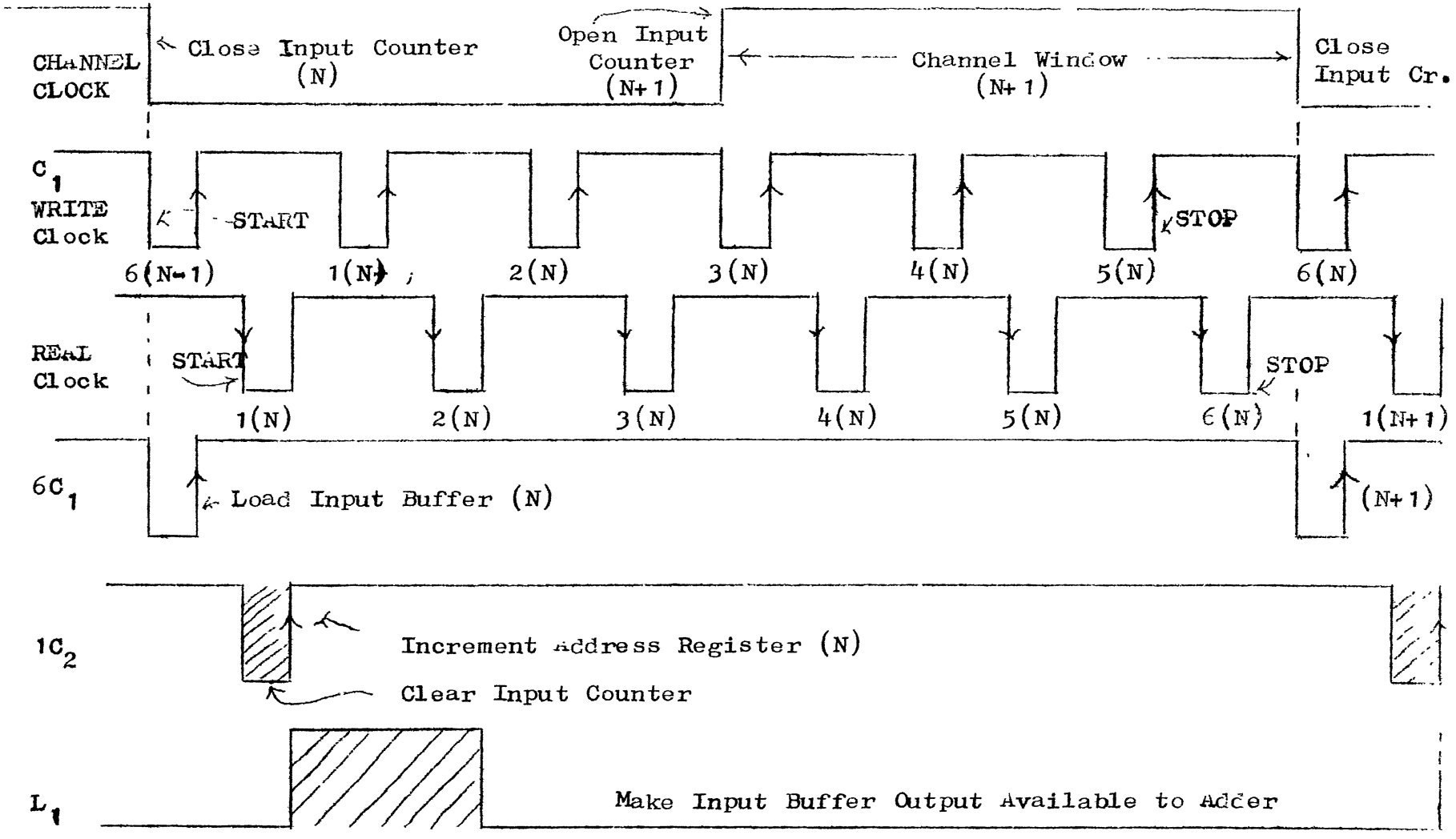

CHANNEL CLOCK
Close Input Counter (N)
Open Input Counter (N+1)
Channel Window (N+1)
Close Input Cr.
C1 WRITE Clock
START
STOP
6(N-1)
1(N)
2(N)
3(N)
4(N)
5(N)
6(N)
REAL Clock
START
STOP
1(N)
2(N)
3(N)
4(N)
5(N)
6(N)
1(N+1)
6C1
Load Input Buffer (N)
(N+1)
1C2
Increment Address Register (N)
Clear Input Counter
L1
Make Input Buffer Output Available to Adder

Fig. 2.3(a)

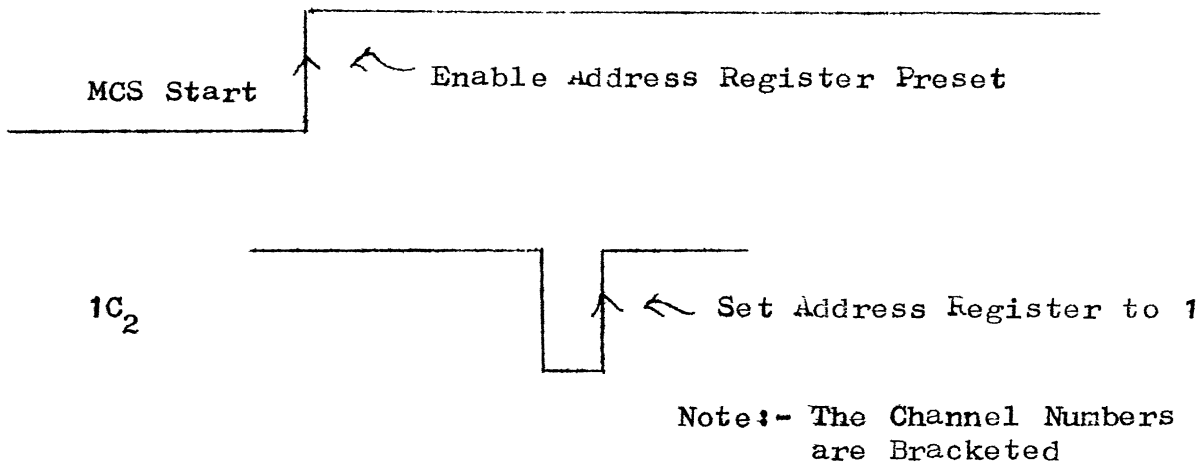

MCS Start
Enable Address Register Preset
1C2
Set Address Register to 1
Note:- The Channel Numbers
are Bracketed

Fig. 2.3(b)

Another important function of the Control Logic is the identification of different channels. This is achieved by running a counter in synchronism with the channel advance of the memory shift register. Clocking this counter with $1C_2$ ensures that at any time the digit at the memory output belongs to the channel number read by the counter. The channel just after the MCS start is to be tagged as the first channel and hence the MCS start should enable the preset of this counter. This is dealt with in more detail in Chapter 3. We will henceforth refer to this counter as Address Register, as it gives the address of the channel being currently processed.

2.5 The Arithmetic Unit

This basically is a BCD adder. The input count is added to the L.S.D. of the Corresponding Channel. The function is explained in the timing diagram of Fig. 2.3. Resulting carry if any, is stored in a delay element and taken care of in the addition of the 2nd L.S.D. This procedure is repeated till the M.S.D. As we do not visualise any Channel Count overflow, the delay element need not be cleared before the next channel starts. The hardware required to Counter Channel overflow if any, is presented in Chapter 6.

2.6 Dynamic Versus Static Shift Registers

Having decided in favour of MOS shift registers the next choice we have to face is dynamic or static? The static MOS does not need any refreshing recirculation and hence there is no lower limit whatsoever on the frequency range, where as the dynamic MOS always needs recirculation and the frequency of circulation can not fall below a certain value. The power consumption of the static MOS definitely is lesser than that of dynamic as there need not be any circulation (power consumption is a function of circulation rate). So purely from physical behaviour, the static memory does have an upper edge. But the most effective factor that is in favour of the dynamic memory is the cost. Comparing the cheapest available static memory with a dynamic memory of double the frequency range, the cost ratio per bit is more than 2.5 to 1.

For the sake of the numbers we compare the price in 1972 December of these memories.

Chip	Type	Frequency	Bits	Voltage	Cost
TMS 3101	Static	0-2.5 MHz	2 x 100	Low threshold	$ 10.5 (1-9) $ 9.6 (10-24)
TMS 3401	Dynamic	20KHz-5MHz	512	"	$ 5.6 (25-99) $ 5.0 (100-)

The present system has an option for 256 and 512 or more channels. Even for 256 channels the extra cost incurred on account of static memory would be $ 9.6 x 12 = $ 115.2.

Let us now have an overall cost comparison between the two posibilities. One has to consider the fact that additional circuitry are needed to obtain digital display from a dynamic memory. If static memory is used, we can obtain a static digital display of the channel number and the Channel Count directly from the Address Register and the memory output respectively. Even with a dynamic memory, digital display would be possible if the display can be programmed to be synchronous with the memory circulation. However, the required minimum rate of memory advance, for any dynamic memory available in the world market today, is too high to permit such a synchronism. A dynamic memory would therefore have to be accompanied with a "Channel Selector", which would bring out the

Channel Count corresponding to any channel of interest, from the memory and make it available for visual display. This will need a static Buffer Memory having the same capacity as one channel (6 digit BCD), a Set Register to contain the desired channel number and a Coincidence Unit to detect the coincidence between the Set Register and the Address Register. In addition an arrangement to advance the address in the Set Register at an appropriate rate will also be necessary for generating outputs for a typewriter. Moreover, the Set Register should be a counter for sequential display.

Additional cost for dynamic memory would be as follows:

Cost of the Set Register, needing 3 Decade Counter @ $ 2 each = $ 6

Cost of Buffer Memory needing 6 parallel 4 bit Registers @ $ 2 each = $ 12

Cost of the Coincidence Unit, needing 3 Quad exclusive OR gates and 1 Quad NAND gate = $ 2

Total additional cost = $ 20

From the above discussion we see that the choice of dynamic memory results in a net saving of $ 95 for 256 channels. This saving is increased to $ 210 for 512

channels. The saving shoots up further with further expansion of the memory as demanded by the Specifications.

Another important drawback of using static memory is the fact that since only a single register is used, data intake would necessarily have to be inhibited during the Display mode. It is true that the back up power required for static memories would be almost half that of dynamic but as this power forms a very little portion of the net back up power, that includes a part of Control Logic circuitry, this is hardly an advantage.

Considering all these factors we opt for the dynamic memories. On the basis of availability we have selected TMS 3401, 512 bit serial dynamic shift register, which was the chip with the highest bit density available at the time. This chip perfectly meets the frequency requirements stated in Section 2.3.

2.7 The Display Unit

Part of the Display Unit has already been explained in Section 2.6. It consists of a 3 digit BCD counter - called Set Register - a Coincidence Unit to check the coincidence of the Set Register with the Address Register, a Buffer Memory to which the memory output

is transferred whenever this coincidence occurs and a programmable slow astable to advance the Set Register. It is to be noted that the Set Register should be set to 1 after the highest Channel number in the present case 256.

2.7.1 Nixie Display:

This would need 9 BCD/10 line converters and Nixie drivers, 3 at the Set Register and 6 at the Buffer Memory outputs. The technique of coincidence also demands that the Address Register too should be a 3 digit BCD Counter. This digit number may increase for an increase in total Channel number.

2.7.2 CRO X - Y Display:

The 6 digit BCD output of the Buffer Memory can be fed to the Y axis through a D/A converter. A ramp can be generated for the X axis. This ramp should be initialised to zero just after the highest channel number (256).

2.7.3 Type Writer Output:

There should be a serial output of digits starting from MSD of Set Register and ending with LSD of the Channel Count in the Buffer Memory. A Shift Signal should be incorporated just preceding the Channel Number and the

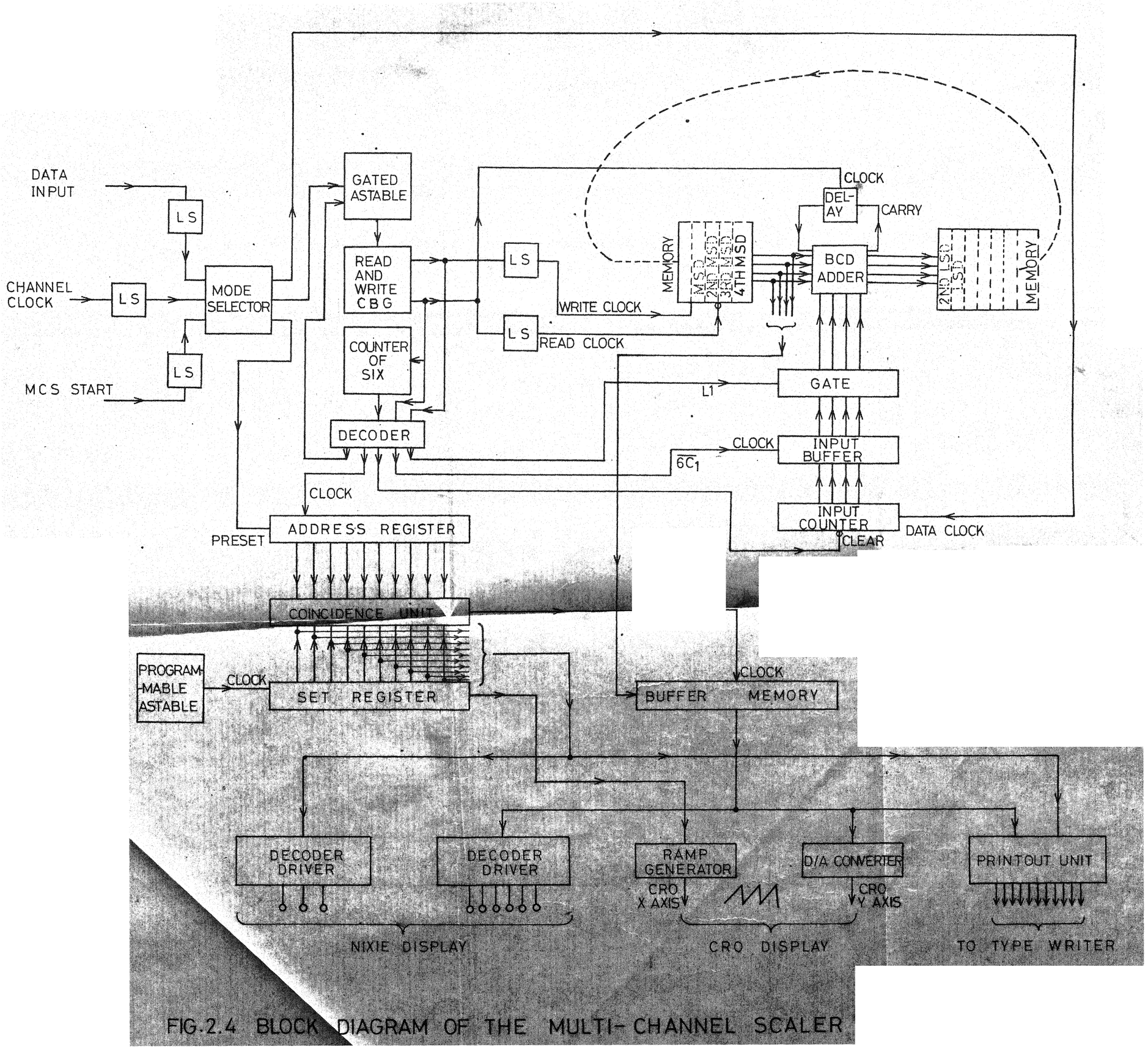


FIG.2.4 BLOCK DIAGRAM OF THE MULTI-CHANNEL SCALER

Channel Count. After a fixed number of channels (say 6) a Return signal must be generated to start the next line.

Thus through Section 2.1 to 2.7 we have developed a detailed version of the entire system required. Fig. 2.4 presents a block diagram of the same, based on the above discussion.

CHAPTER III

CONTROL LOGIC AND THE ARITHMETIC UNIT

The chapter deals in detail with the hardware required for the Control Logic and the Arithmetic Unit. An attempt is made to explain the main hardware features of every block of these units presented in the block diagram of Fig. 2.4.

3.1 Gated Astable

The Gated Astable running at twice the memory advance frequency feeds pulses to the two CBGs one for Read and other for Write.

As explained in Section 3.7 on the basis of eqn. (1) and (2) of the same, we select T_1 = 4 microseconds

T = 15.5 "

The C_1, R_1 values are based on the approximate formulae

$$T_1 \cong 1.08\ C_1R_1$$

$$T_2 \cong 1.08\ C_2R_2$$

The Channel Clock controls the astable through the gate pulse G. To enable the circulation to be maintained in the memory during the FREE mode. This is ensured

by making the astable Free Running during FREE mode which is indicated by Logic Signal IC = 1. IC stands for Independence Command. The above requirement are realised by making $G = \overline{IC} \cdot L_6 \cdot \overline{C}$

The final overall circuit of the gated stable is shown in Fig. 3.1.

3.2 Read and Write CBGs

Clocks C_1 and C_2 for Read and Write respectively are generated as shown in Fig. 3.2, as per following expressions:

$$C_1 = A \cdot Q$$

$$C_2 = A \cdot \overline{Q}$$

Exact timing relations are shown in Fig. 3.3. $1C_2$ and $6C_2$ make available at the memory output the LSD and MSD respectively. $1C_1$ and $6C_1$ Write the LSD and MSD in the memory. As a digit has to be accessed, up dated and stored back in the memory the Read Clock must precede the Write Clock for the same digit.

As the LSD should appear after the Channel Window is closed, the $\overline{1C_2}$ occurs after the negative edge of the Channel Clock.

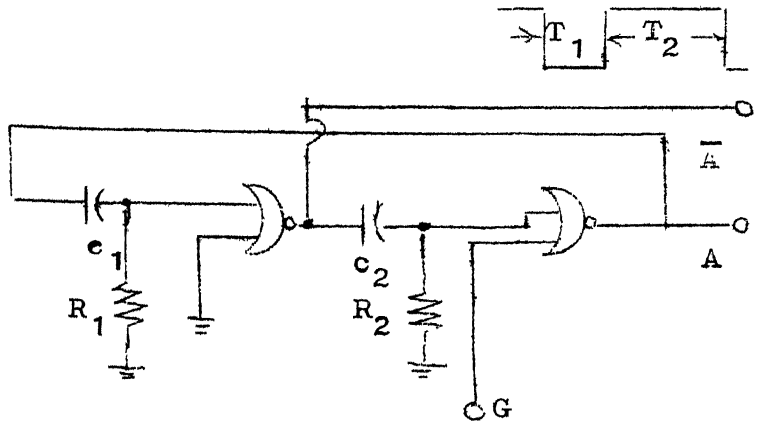


Fig. 3.1 THE GATEL ASTABLE

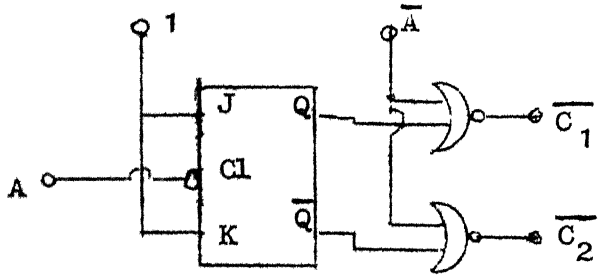


Fig. 3.2 THE REAL AND WRITE
CLOCK BURST GENERATORS

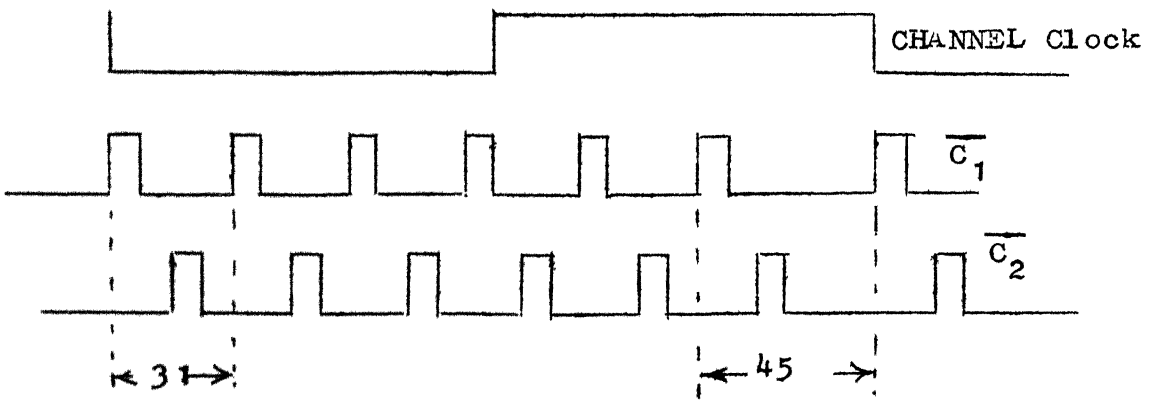


Fig. 3.3 THE TIMING RELATIONS

3.3 The Counter of Six

For operations of Section 3.1 and 3.2 we need a six state counter. This is negative edge triggered and $\overline{C_2}$ is used as clock as explain in Section 2.4. This counter is used with a decoder and hence a cyclic code is followed as given below.

Q_3	Q_2	Q_1	Line
0	0	0	L_1
0	0	1	L_2
0	1	1	L_3
1	1	1	L_4
1	1	0	L_5
1	0	0	L_6
0	0	0	L_1

3.4 The Decoder

A decoder is used to decode lines L_1 and L_6 which are required for the control function, as per the following expressions:

$$L_1 = \overline{Q_1} \cdot \overline{Q_3}$$

$$L_6 = \overline{Q_2} \cdot Q_3$$

$\overline{6C_1}$ and $\overline{1C_2}$ which are required for operations depicted in Fig. 2.3 are also decoded.

$$\overline{6C_1} = L_6 \cdot \overline{C_1}$$

$$\overline{1C_2} = L_6 \cdot \overline{C_2}$$

3.5 The Level Shifters

The Level Shifters are used for the Channel Clock, the MCS start and the Data. They also serve as a safeguard for the MCS against any damage due to fault in the accompanying instruments, that generate these signals.

The MCS and Data Level Shifters are ordinary ones. The Level Shifter for the Channel Clock also serves as an invertor.

The Clocks for the memory are obtained by inverting the CBGs outputs. These need special design considerations. The MOS memory basically is a high capacitive load. TMS 3401 offers worst case capacitance of 280 pF/chip. The maximum transition period at a clock edge (+5 V to -12 V) is 1 microsecond. Designing for a transition period of $\frac{1}{2}$ microsecond for 512 channels (24 chips) the source and sink current requirements will be as follows:

$$I = C \times dv/dt$$

$$= (24 \times 280) \times ((5 + 12)/\tfrac{1}{2})$$

$$= 300 \text{ mA approximately.}$$

This high current switching is ensured by using two output switching transistors in complementary mode as shown in Fig. 3.4.

3.6 The Address Register

As explained in Section 2.7 the Address Register is a three digit BCD counter. It is realised by using 3 Decade Counters (EC 790) in tandem. These counters are negative edge trigged. To match the requirements of timing diagram of Fig. 2.3 the clock to this counter has to be $\overline{1C_2}$.

3.6.1 Presetting the Address Register:

The Channel number varies from 1 to 256. The first channel is defined as the one whose window opens just after the positive edge of the MCS start pulse. As the MCS start is derived by scaling down the Channel Clock in the Spectrometer its edges coincide with either the positive or the negative edge of the Channel Clock. The TTL delays of the Scaler and the Level Shifters

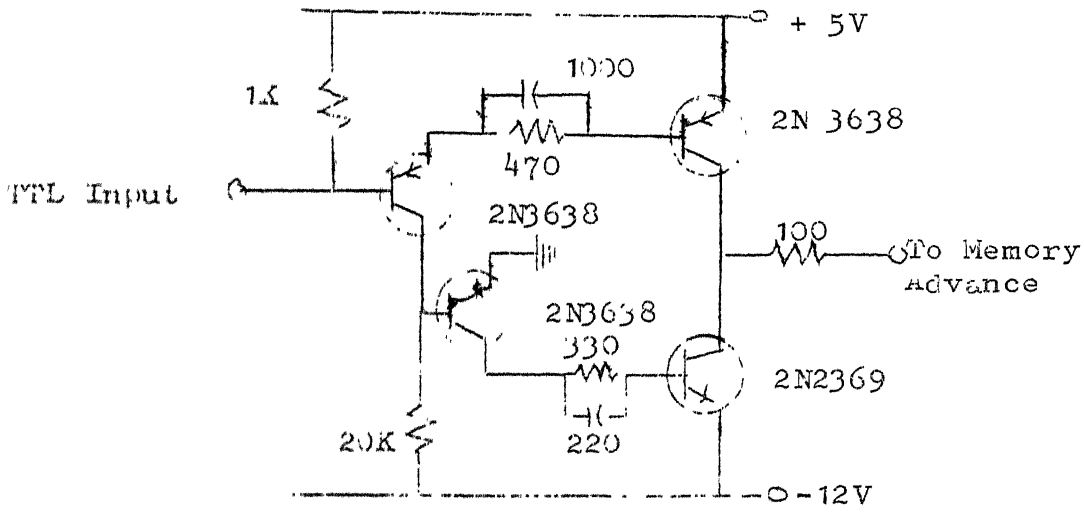


Fig. 3.4 LEVEL SHIFTER FOR MEMORY CLOCK

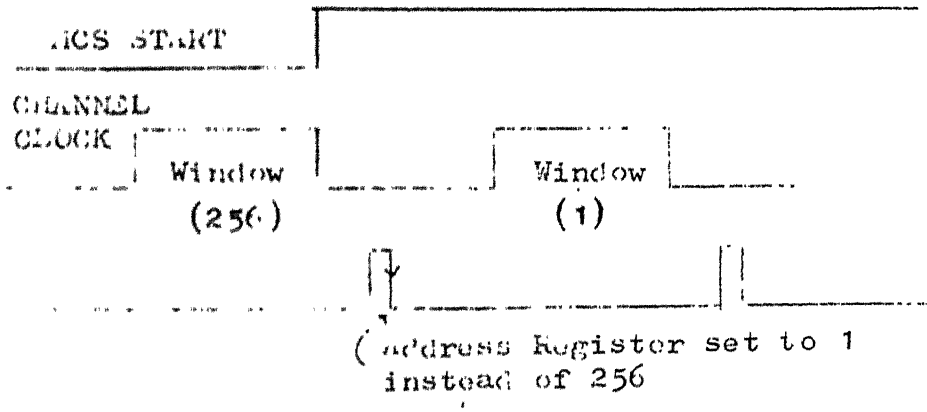


Fig. 3.5(a) SETTING BY $\overline{IC_2}$

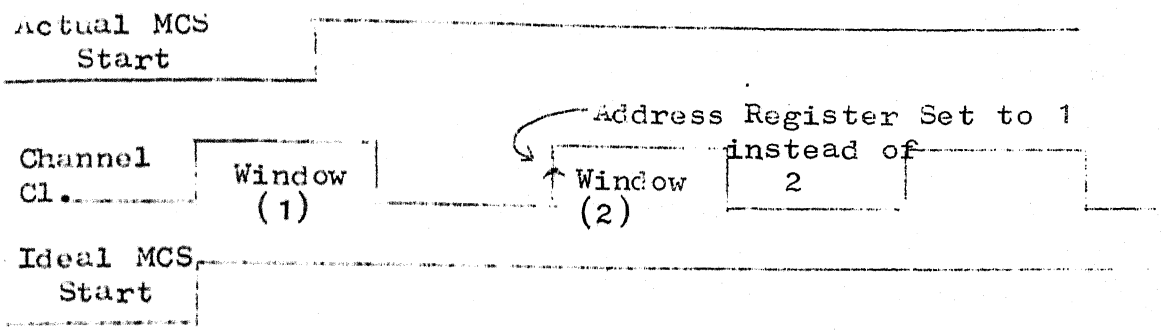


Fig. 3.5(b) SETTING WITH POSITIVE EDGE OF CHANNEL CLOCK

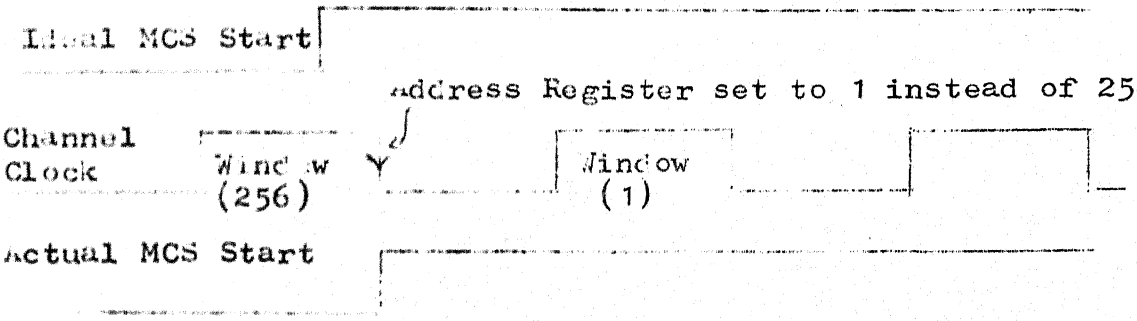


Fig. 3.5(c) SETTING WITH NEGATIVE EDGE OF CHANNEL CLOCK

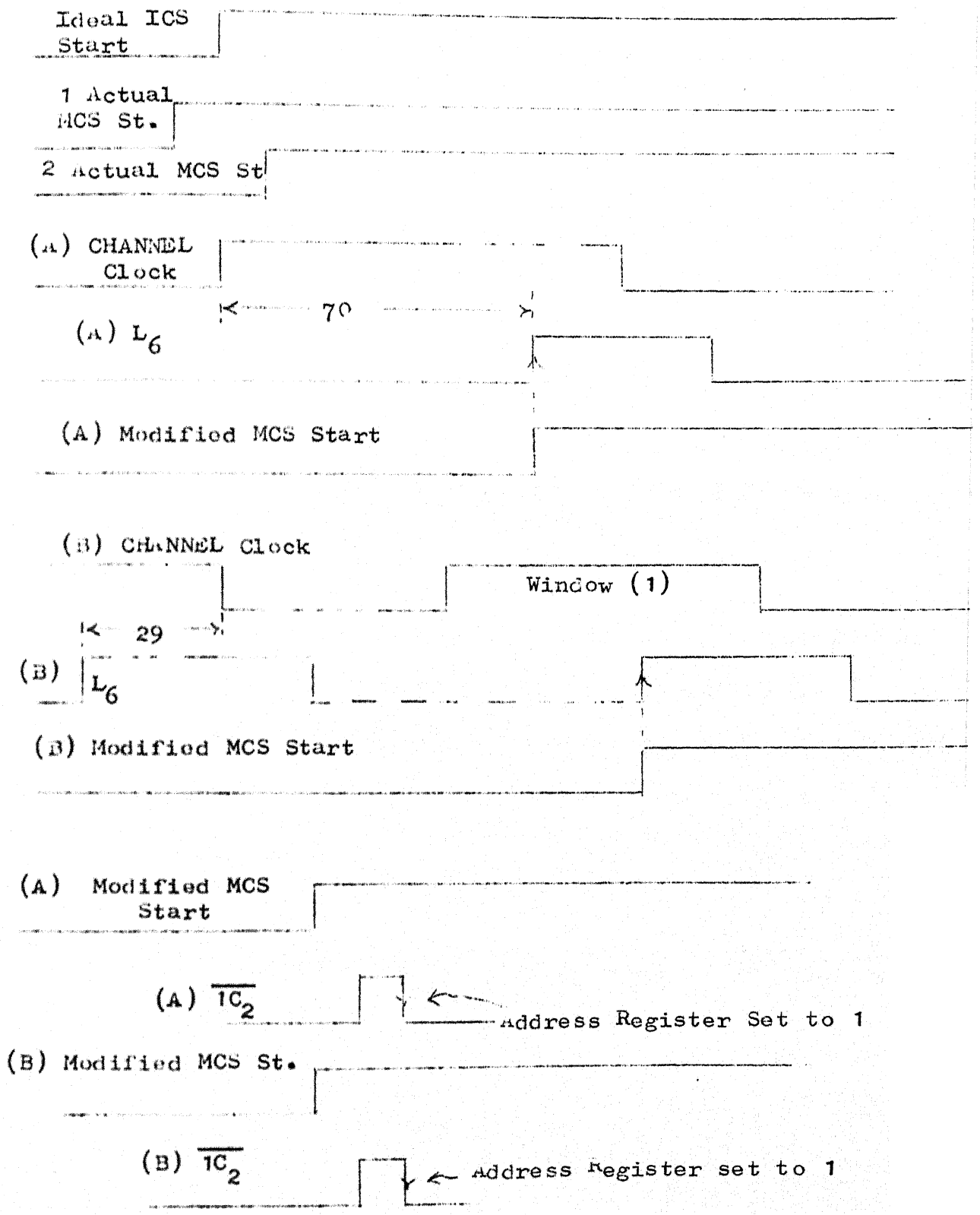


Fig. 3.5(d) THE PROPER WAY OF PRESETING THE ADDRESS REGISTER

delays may add up to hundreds of nanoseconds and hence the MCS start may lead or lag the corresponding edge of the Channel Clock by so much time. Taking into consideration this fact we discuss in Fig. 3.5 the merits of various methods of presetting the Address Register.

The EC 790s have no provision for presetting to 0001_t. As the Address Register has to be set to 1 after 256 we actually set it to 0 for an insignificant time between these channels. The Address Register is cleared between the positive edge of $6C_1$ and negative edge of $1C_2$ of channels 256 and 1 respectively. It is clear that the time between the positive edge of $6C_1$ and the negative edge of $1C_2$ of the immediately following channel is of no consequence as the Write Operation is over and fresh outputs are yet to arrive. The Address Register is clocked to 1 with the negative edge of $\overline{1C_2}$ of channel 1 as demanded. (Fig. 3.6)

3.7 Mode Selector

Switching from the CLOCK mode to the FREE can be done manually by putting IC = 1 and letting the astable of Fig. 3.1 run freely.

Switching from FREE mode to CLOCK mode can be done only after ensuring 2 conditions:

(A) The negative edge of the Channel Clock should not be far displaced from $6C_1$ at the start, else the data in memory will be lost as explained in Fig. 3.7.

(B) The MCS start pulse should coincide with 256 channel to ensure synchronism between fresh data and the stored one.

The first condition can be satisfied by ANDing a monostable pulse triggered by the negative edge of Channel Clock with $\overline{6C_1}$. Output if any, indicates matching. This method has to account for two extreme cases.

(1) The clock negative edge leads the positive edge of $\overline{6C_1}$ by a time "b".

(2) The clock negative edge lags the positive edge of $\overline{6C_1}$ by a time "a".

The method demands a = width of $\overline{C_1} = T_1$ (Fig.3.1). This puts a restriction on the Read and Write Clocks C_1 and C_2. The conditions for faultless operations as discussed in Fig. 3.8 are as follows:

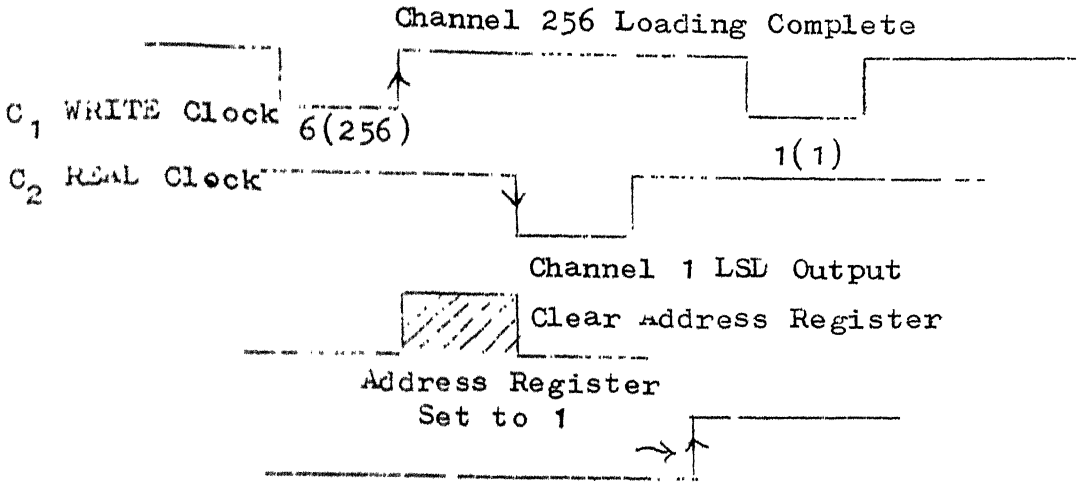


Fig. 3.6 PRESETTING ADDRESS REGISTER

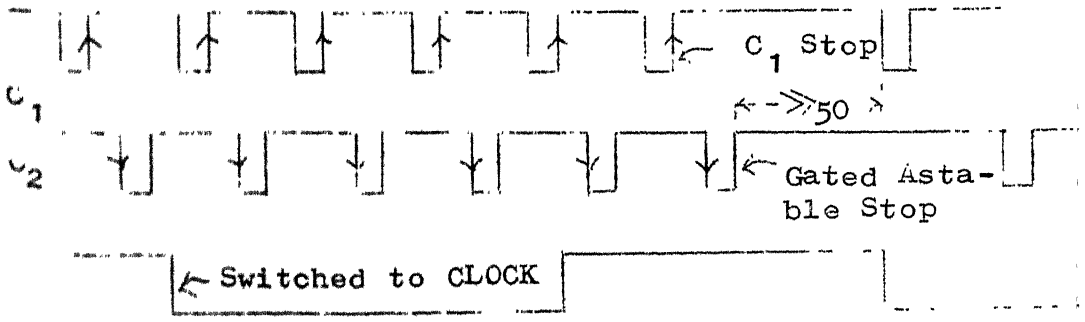


Fig. 3.7 INDISCRETE SWITCHING TO CLOCK MODE

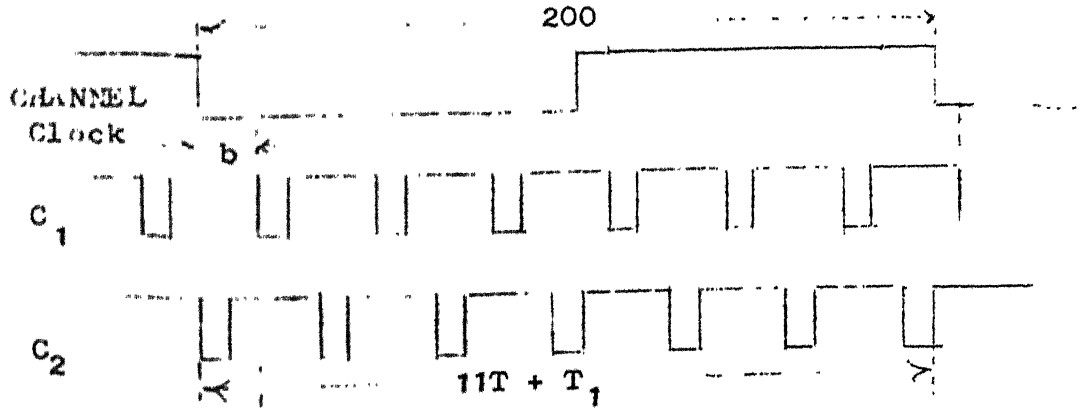


Fig. 3.8

For 5 KHz Channel Clock

(1) $200 - b - 11T - T_1 \leq 50$ microseconds, where 50 microseconds is maximum time gap allowed between C_1 and C_2.

2) $11T \leq 200$ microseconds.

Condition 2) is redundant as we have in normal operation

$$11T + T_1 \leq 200 \text{ microseconds} \quad \ldots\ldots\ldots (2)$$

any values that satisfy (1) and (2) can be used for generating the astable pulses of Section 3.1.

after selecting T and T_1 as per equations (1) and (2) we satisfy conditions (A) and (B) by the hardware shown in Fig. 3.9.

The clock of the D FF is pulsed only if the $\overline{6C_1}$ just after the positive edge of MCS start overlaps with the monostable triggered by the negative edge of the Channel Clock. The D input of the FF is high only when 256 channel is at the memory output. If the occurence of the 256th channel is coincident with the clock of the D FF it is clear that (A) and (B) are satisfied. The coincidence also sets the FF to logical 1 and IC = 0 which switches the clock back to CLOCK mode. The whole operation is explained in Timing diagram of Fig. 3.10.

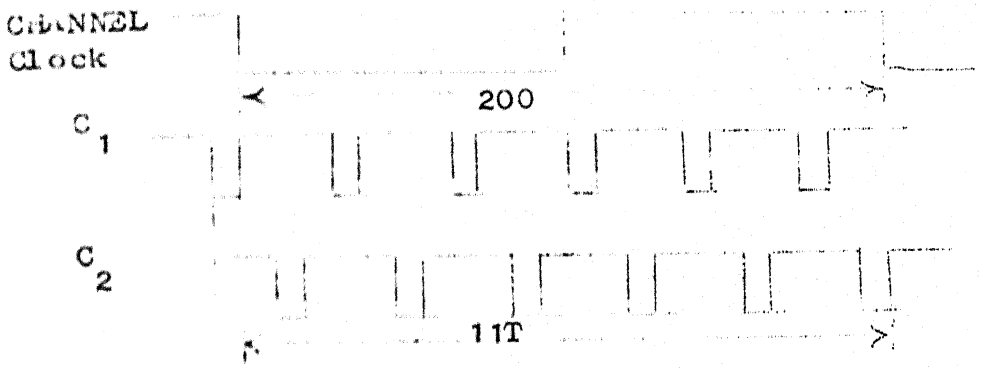


Fig. 3.8(b)

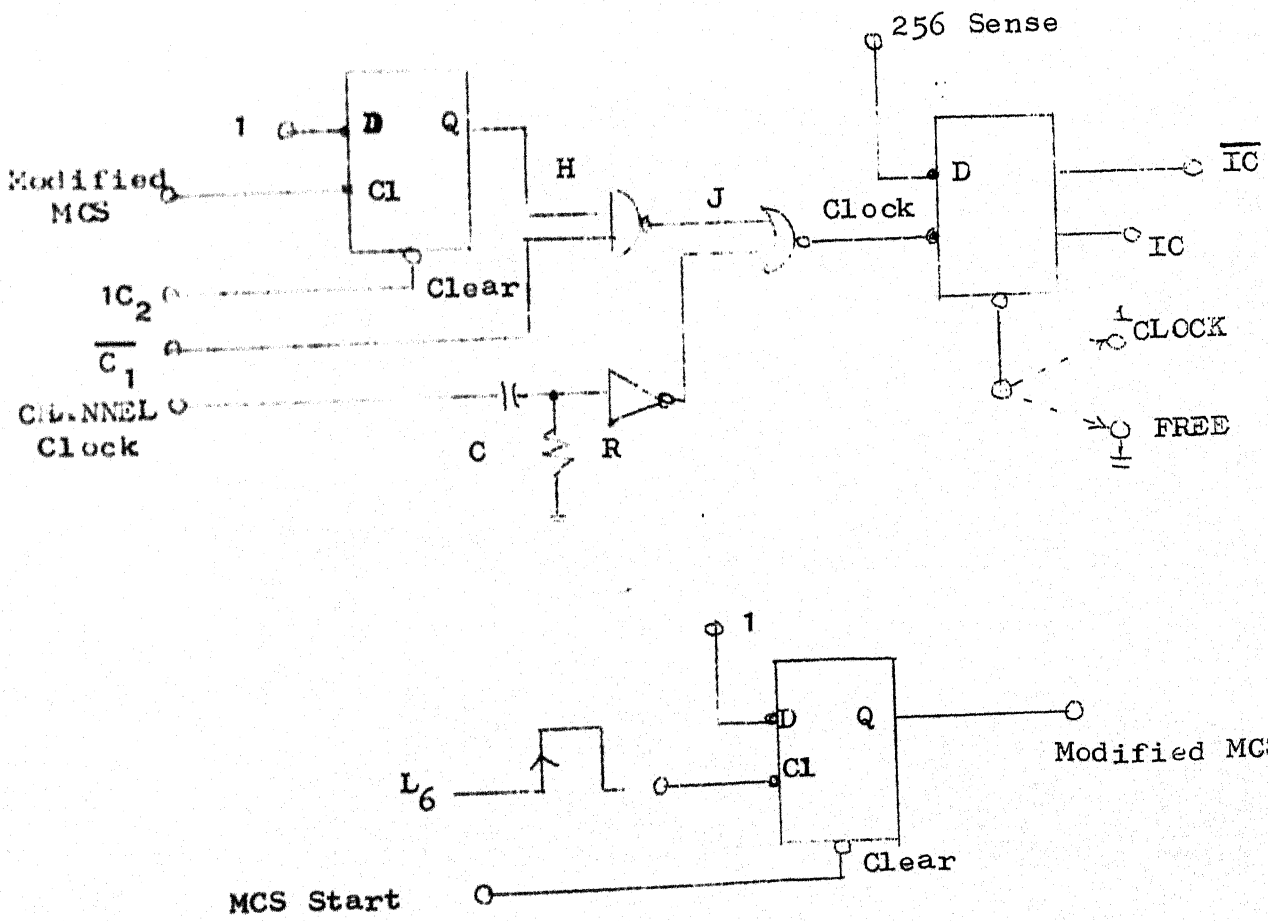


Fig. 3.9 MODE SELECTOR

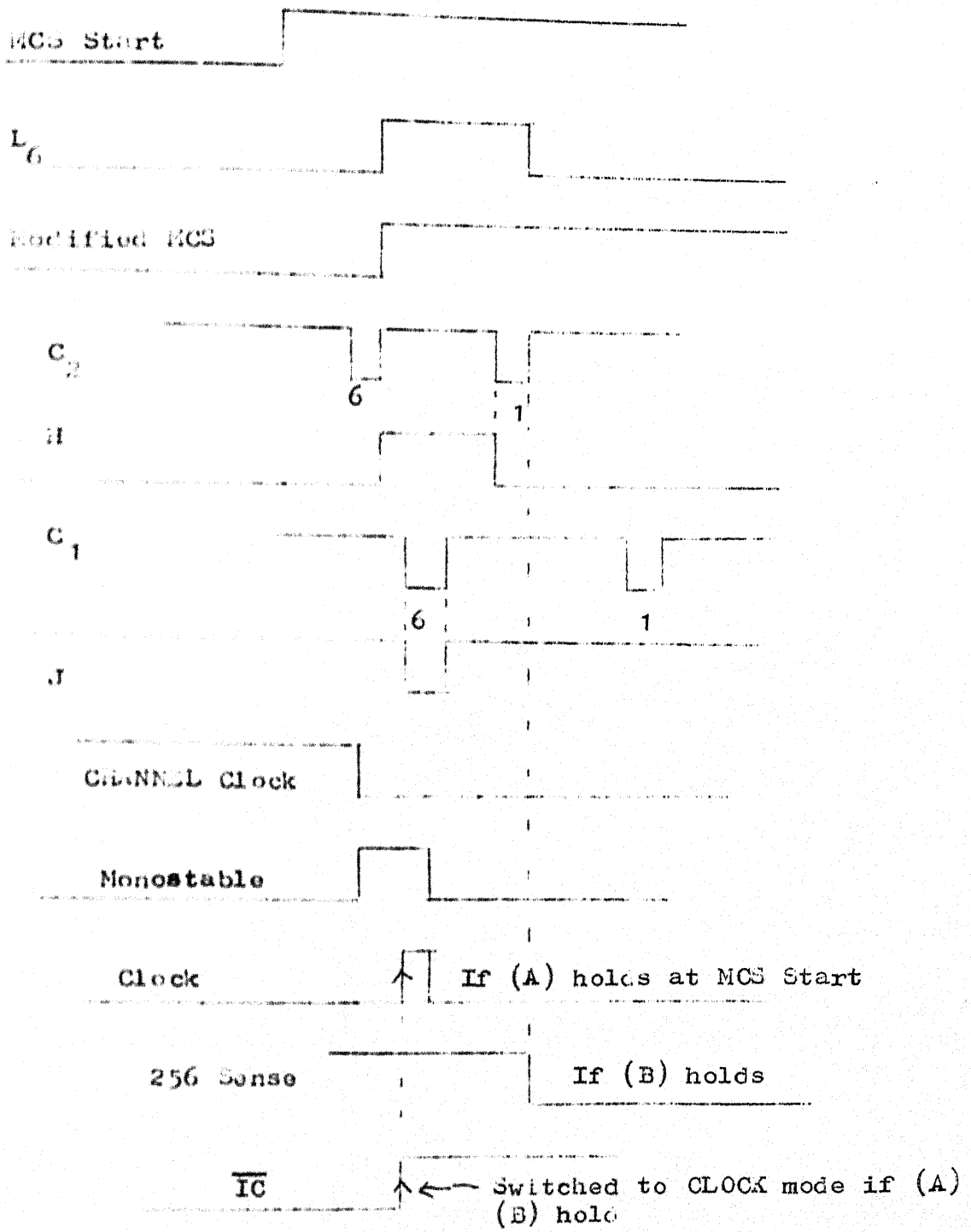


Fig. 3.10 TIMING DIAGRAM FOR MODE SELECTOR

3.8 The Input Counter

The Input Counter is a simple binary counter with a clock which is referred to as the "Data Clock".

Data Clock = IC + $\overline{C}$ + $\overline{DATA}$

This ensures

(1) That the Data clock is 1 when FREE mode is on

(2) The Data Clock is 1 when Channel Clock is negative.

Thus there is no counting when IC = 1 i.e. FREE mode is on or when the Channel Window is over.

The Input Counter is cleared by $1C_2$ to ensure the timing relations shown in Fig. 2.3.

3.9 The Input Buffer

This is just a parallel 4 bit register. A single EC 795 chip has been used. After the channel window is closed the data is transferred to the Buffer on the negative edge of 6 $\overline{C_1}$.

3.10 The Gate

The function of this block is just to make data available to the adder only when the LSD is present at the memory output. This therefore consists of 4 2-input

AND gates, with L_1 as the control input common for all the four gates.

Figure 2.3 explains the working on the CLOCK mode.

3.11 The BCD Adder

This consists of two binary adders with a provision for delaying the carry till the next digit occurs, as shown in Fig. 3.11. Obviously $\overline{C_2}$ is used as a clock of the positive edge triggered delay element. The output of the first adder is binary and the second adder merely serves to convert the result into BCD by addition of six, if necessary. This is achieved by generating a signal T given by the following expression:

$$T = C_4 + E_4 \cdot (E_3 + E_2)$$

T is connected as the 4 - and 2-- inputs to the second adder.

The Erase Operation of the Unit is dealt with in Chapter 5.

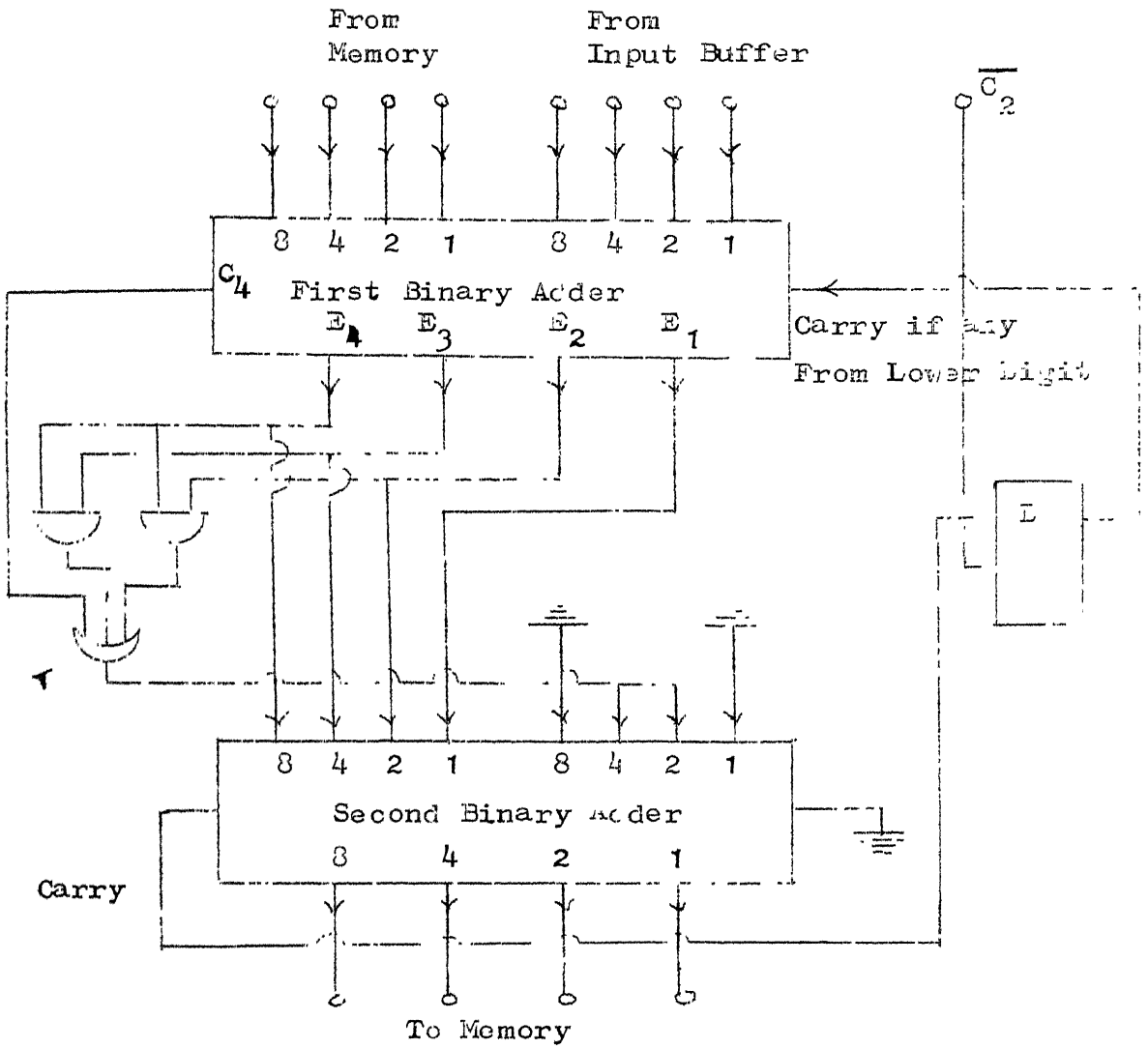


Fig. 3.11 BCD ADDER

CHAPTER IV

THE DISPLAY UNIT

The basic blocks of the display unit have been discussed in detail in Section 2.7. Here we discuss the actual hardware of these blocks through various sections.

4.1 Set Register

This being a BCD counter as discussed in Section 2.7, we simply use 3 Decade Counter chips (EC 790) in tandem. Figure 4.1 shows an arrangement for obtaining a cycle length of 256 without making the count of zero appear on the display. The C_1 R_1 form a monostable that triggers at the positive edge of the clock pulse. The monostable output is of much lesser width as compared to the width of the clock to this Register. This pulse is used as the clear pulse of the sSet Register, after a count of 256. The counter is negative edge triggered. So, the Set Register is set to zero for a very short time of the order of microseconds in between the counts of 256 and 1. Therefore, the count of zero, which has no meaning in this system, is not visible on the display panel. Figure 4.2 explains the same in detail.

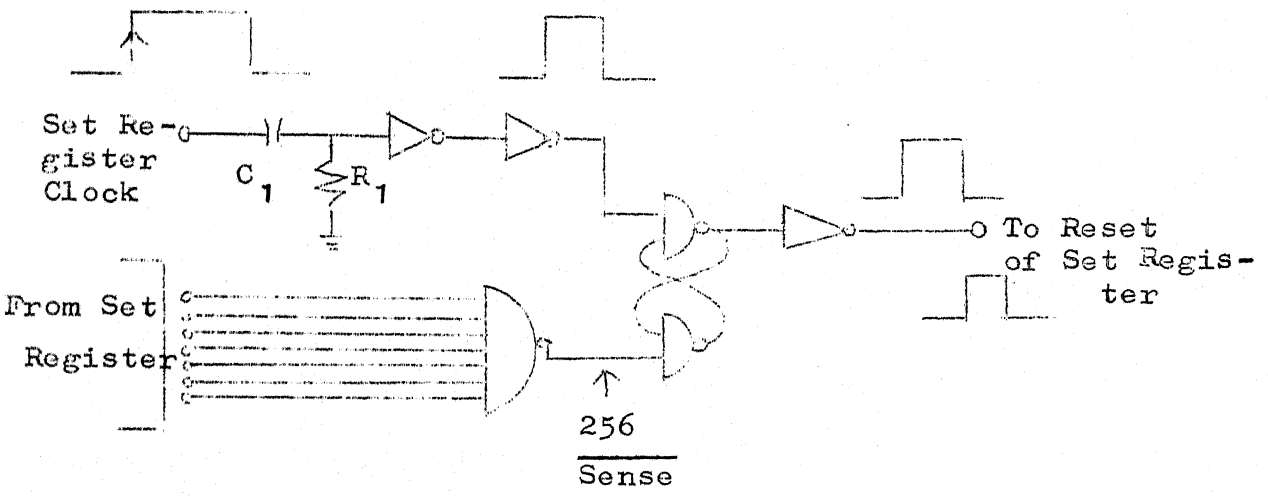


Fig. 4.1 SET REGISTER PRESET

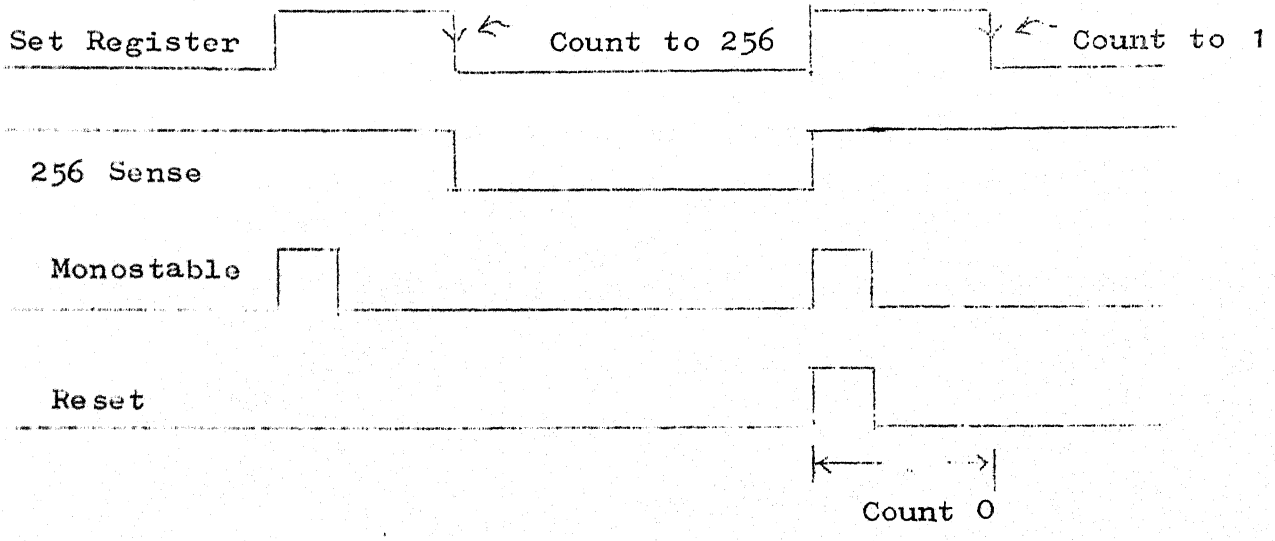


Fig. 4.2 TIMING RELATIONS FOR SET REGISTER PRESET

4.2 Coincidence Unit

We obtain a digit-wise coincidence signal, such that it goes to 1 whenever the corresponding digit of the Set and the Address Registers match. The circuit consists simply of 4 Exclusive OR gates for the four bits and one 4 input NOR gate to obtain the digit coincidence signal. The digit coincidence signals for all the 3 digits are then AND ed to obtain the ultimate Coincidence pulse. This pulse envelops the loading signals for the 6 digits of the channel corresponding to the Set Register Address. These loading signals are obtained as shown in Fig. 4.3 and the Buffer Memory is loaded.

4.3 The Buffer Memory

These are six 4-bit Shift Registers (EC 795) in parallel mode operation. The four Memory output lines (8 - 4 - 2 - 1) are connected to the four inputs of the first 4-bit register, the outputs of which are connected to the inputs of the next 4-bit register and so on. The clock is the coincidence pulse AND ed with $\overline{C_1}$.

4.4 Decoder - Drivers

There are two Decoder Drivers in the system, one for the Set Register and other for the Buffer Memory

contents. The Decoder for the Set Register consists of three EC 745 chips which also drive the three Nixie tubes for the three digit address in the Set Register. Similarly the Decoder Driver for the Buffer Memory consists of six EC 745 chips for the six digit channel count.

4.5 The Programmable Astable

The period of the Programmable Astable which clocks the Set Register has to range from milliseconds to seconds, to cater for different needs of the user. As the period required is large and the duty cycle can be made low, a negative-resistance relaxation oscillator is a convenient choice. The circuit is shown in Fig. 4.4, where an inverter is included to provide TTL compatibility at full fan-out.

The Set Register is advanced by a different astable in the PRINT mode. Hence this astable is inhibited in the PRINT mode by making $\overline{PC} = 0$ which ensures that the C R combination is grounded and the astable is put out of action.

4.6 The CRO X - Y Display

The functional block of the CRO display has already been explained in Section 2.7. Because of the resolution limitations of the CRO scale, we display at a time

any two consecutive digits selected by a CRO Sensitivity Switch on the panel.

The vertical input Y is from a simple D/A converter as shown in Fig. 4.5. We select R and 2R as 1K, 2K; each, .1% and nR = 7.5K, R_1 = 3K
The maximum output d_1, d_2 is 5 x 7.5/6 = 6.25 Volts. pR is chosen suitably to obtain proper amplitude at the output.

Figure 4.6 depicts the ramp generator which is a simple d.c. integrator whose output is set to zero when the Set Register reads 256.

4.7 The Print out Unit

This has to generate the signals for an IBM typewriter to print out channel number and channel count, starting from channel 1 to 256. The channel number and the channel count are available in the Set Register and the Buffer Memory respectively. The functions that this unit has to perform are in the following sequence.

(1) At the start, set the Set Register to 1;
(2) Give a Return Signal to bring the carriage to the first column;
(3) To send the Set Register digits, MSD first, one by one;

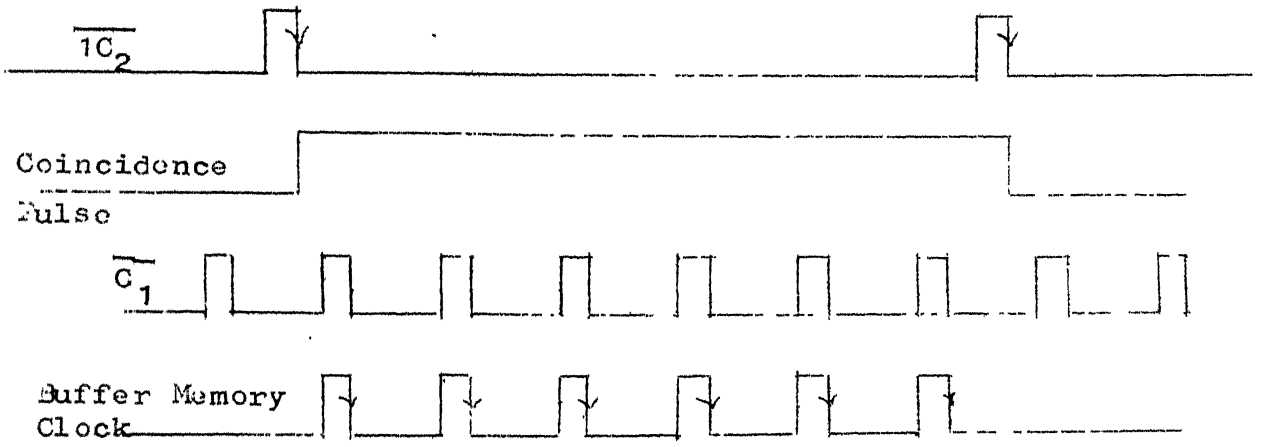


Fig. 4.3 BUFFER MEMORY LOADING SIGNALS

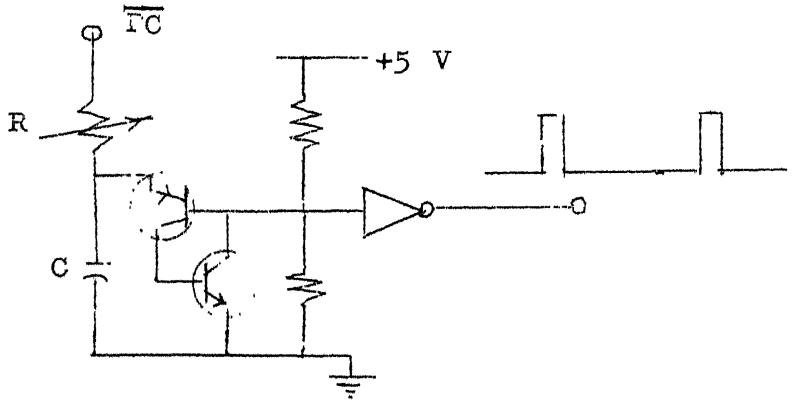


Fig. 4.4 NEGATIVE RESISTANCE ASTABLE

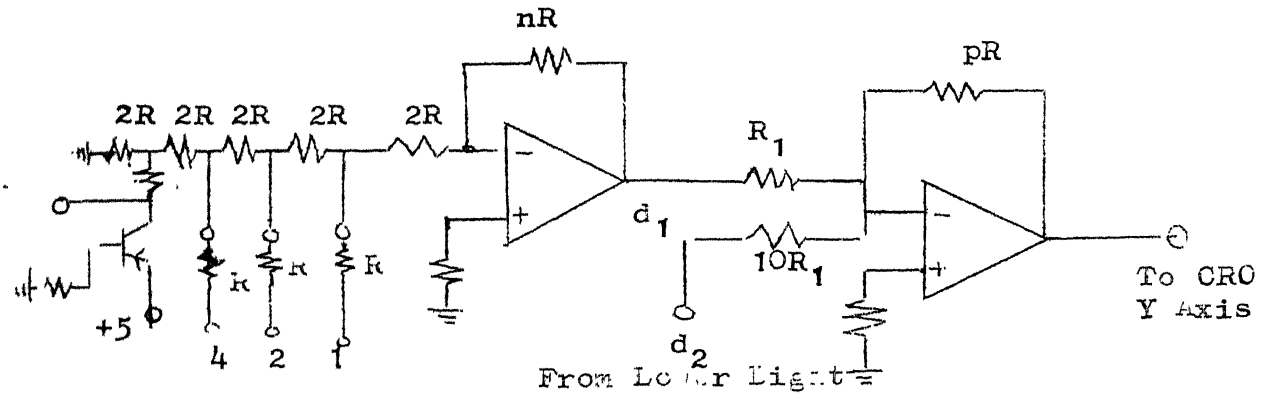


Fig. 4.5 D/A CONVERTER

(4) To send a Shift pulse;

(5) To send the Buffer Memory contents, MSD first, digit by digit;

(6) To check the Set Register reading and stop if the reading is 256;

(7) To return the carriage if the Set Register reading is n, 2n, 3n --------, where n is a predetermined integer (n = 6 has been chosen in the actual circuitry);

(8) To advance the Set Register by 1 and start the sequence again from step 1.

The hardware shown in Fig. 4.7. As the astable required should have a large duty cycle the programmable astable of Fig. 4.4 can not be used. Instead a separate NOR gate astable is employed.

PC refers to Print Command. PC = 0 is ensured at power on. Under this conditions the astable is inhibited and the Print out Unit is off.

The Shift Register is used as a counter-decoder, to generate the 11 lines required for the operations stated above. When PC = 0 the Shift Register is parallelly loaded such that only the first line is on. PC = 1 switches this register in serial mode, and the 11 lines

(M_1 - M_{11}) are enabled sequentially. The functions performed by the 11 lines are given in Table 1.

TABLE - 1

LINE	FUNCTION PERFORMED WHEN THE LINE IS ON
M_1	Shift/Return Signal
M_2	MSD channel number is transferred to typewriter
M_3	2nd MSD " "
M_4	3rd MSD " "
M_5	Shift Signal
M_6	MSD Channel Count
M_7	2nd MSD Channel Count
M_8	3rd MSD " " "
M_9	4th MSD " " "
M_{10}	5th MSD " " "
M_{11}	LSD " " "

The NOR gate astable is so designed that at output A,

T_1 = The optimum time for which the typewriter coil should be energized;

T_2 = The optimum time that should elapse in between any two energization of typewriter coils.

Further gate circuitry is required to ensure the above requirements regarding the 11 signals of Table 1.

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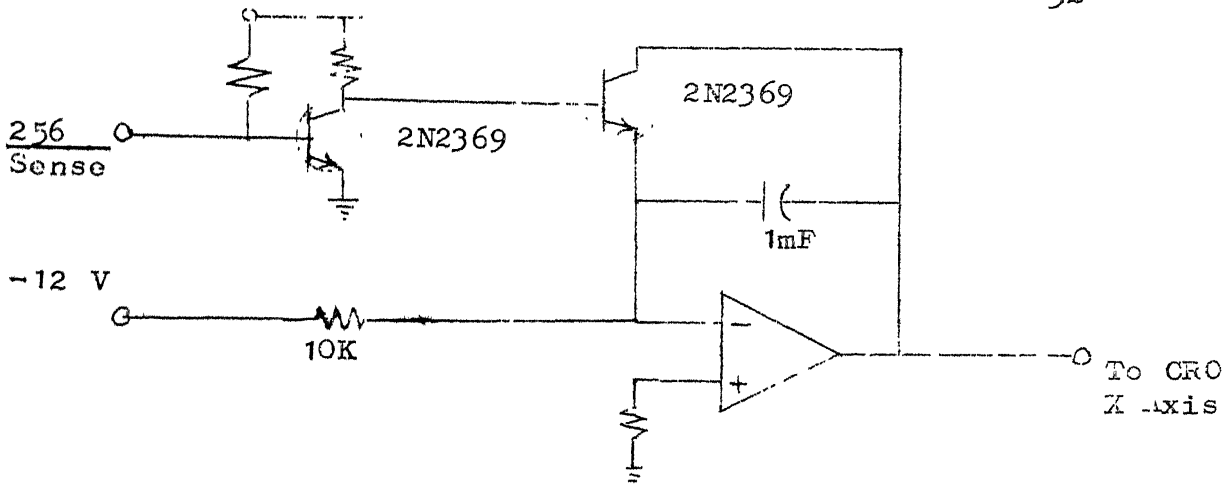

Fig. 4.6 RAMP GENERATOR

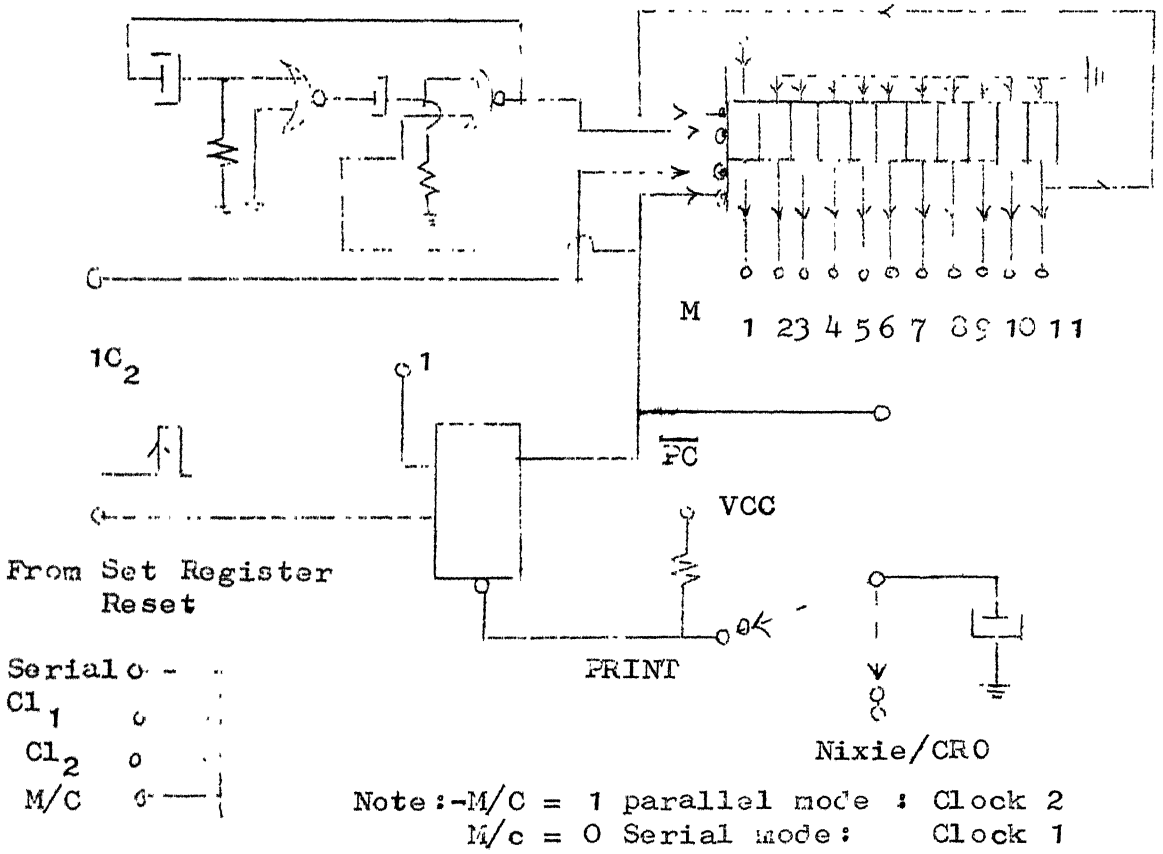

Fig. 4.7 THE PRINT UNIT CONTROL

The Print Unit is switched on by manually putting PC = 1. This also clears the Set Register to ensure that the typing starts from channel 1. At the end of 256th channel a FF is set to ensure PC = 0 and the Print Unit is switched off.

CHAPTER V

SAFEGUARD AGAINST POWER FAILURE

A typical Mossbauer Spectroscopy experiments runs for tens of hours. Special arrangements have to be made to ensure that the data is not lost in the midst of an experiment because of a Power Failure. The chapter deals with the hardware utilised to ensure safeguard against such a power failure.

We are using the MOS memory which is inherently volatile. Hence backup power has to be supplied to the Memory Unit to ensure that the data is preserved in case of power failure. We give this backup by permanently connecting DC batteries to the power supply through diodes; the battery voltages should not be more than the minimum unregulated voltage output of the power supply, since otherwise there would be a drain on the back up even when the line power is on.

The dynamic memory used, demands minimum rate of circulation. Hence memory advance pulses have to be provided even during the power failure. This demands that atleast the part of the Control Logic should be ON during back up. Our efforts would be to minimise the circuits of

of the Control Logic that have to be supplied with back up power so as to reduce the drain on the DC batteries as much as possible.

Power Failure may put off the Mossbauer Spectrometer and hence the Channel Clocks and the MCS start pulse may not be available. Moreover these pulses have to be completely ignored by the MCS so as to take care against any possible transient which may be generated in the Spectrometer due to power failure.

From the above discussion it is clear that the MCS should be automatically switched on to the FREE mode as soon as the power fails. This will also ensure memory circulation during the back up. Hence the Gated Astable, the CBGs and the memory Level Shifters have to be supplied with back up power.

Automatic switching to the FREE mode is ensured as follows: The D FF of the Mode Selector of Fig. 3.9 is not supplied with the back up. Hence the output IC being a TTL output goes to 1 as soon as the power fails. Please note that IC = 1 is basically a command to switch to FREE mode. To take care of the transient that may be generated in IC due to power failure we have the circuit shown in Fig. 5.1.

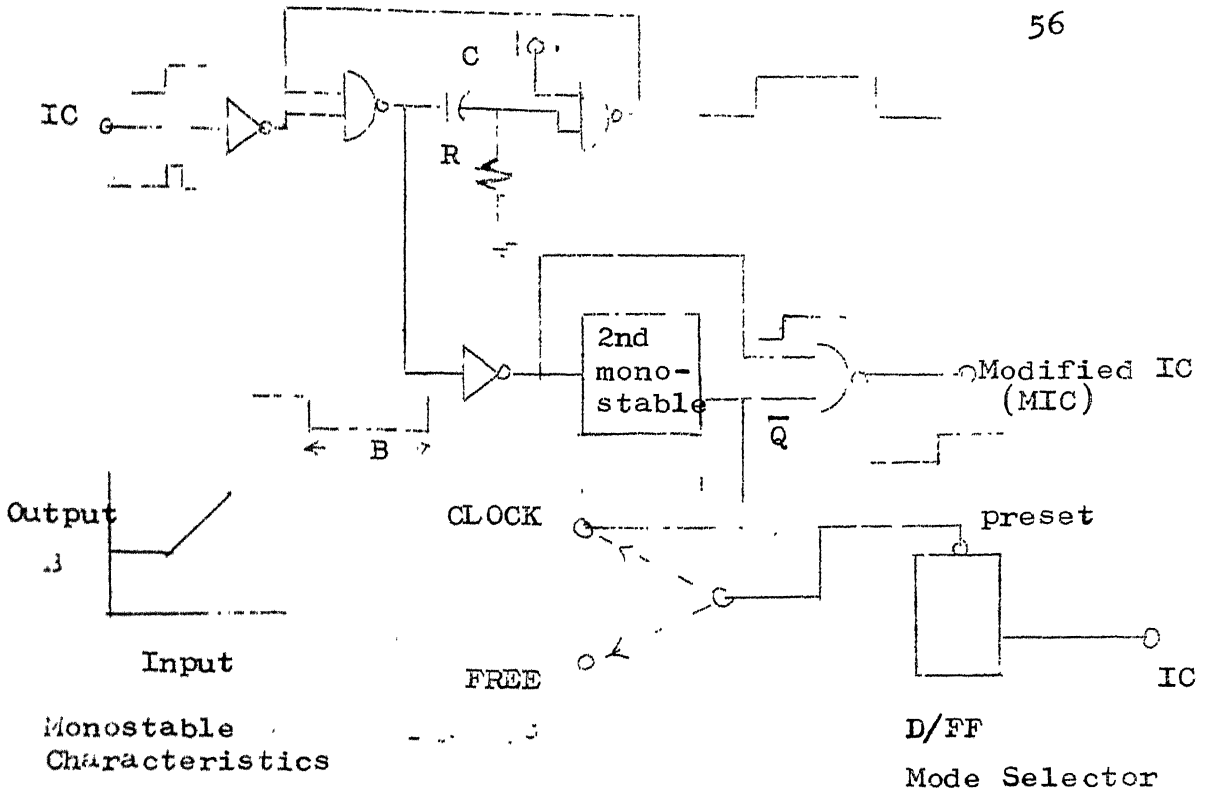

Fig. 5.1 Automatic Switching to FREE Mode on Power Failure

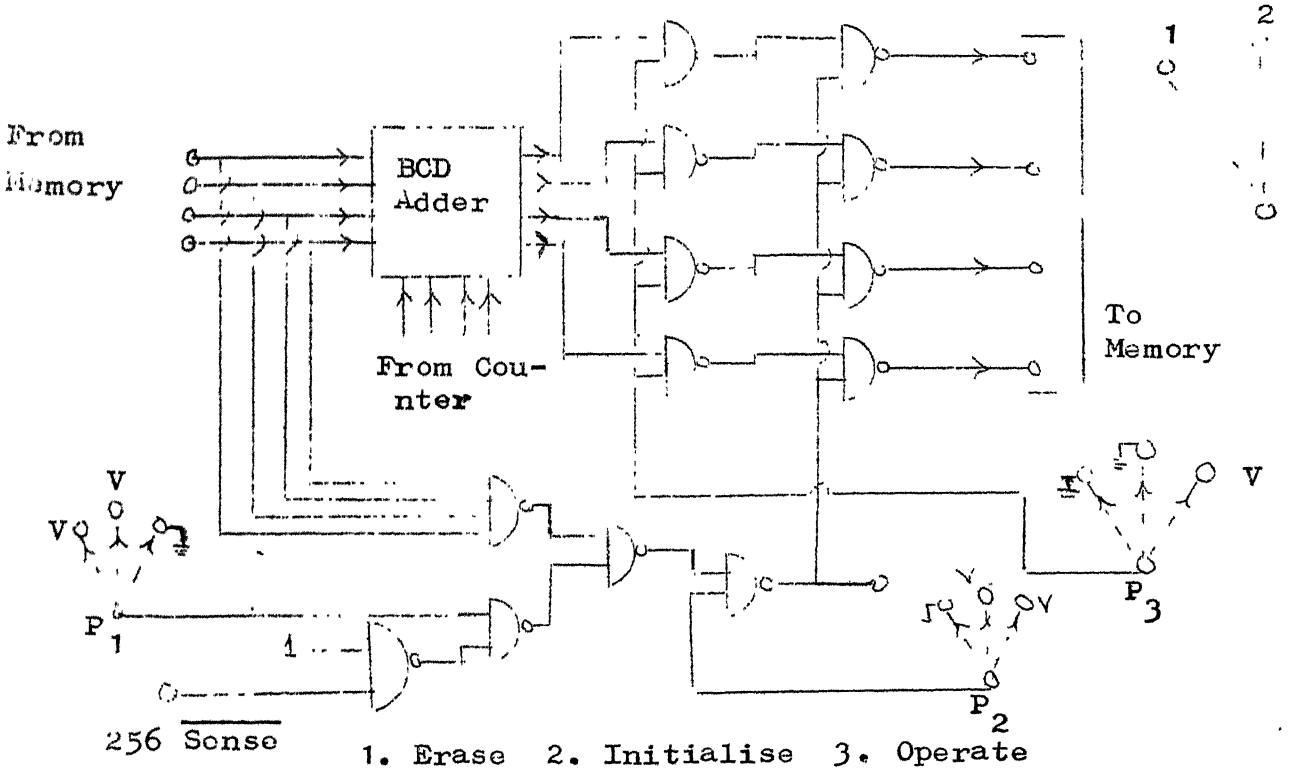

Fig. 5.2 CHANNEL TRACKING

The C R Combination forms a NANL gate monostable whose characteristics is shown in the figure. The positive edge of the monostable output pulse switches on the second monostable whose output pulse is of 40 second duration. The Modified IC (MIC) goes to 1 as soon as there is a transition from 0 to 1 of $\overline{IC}$. Once set to one the MIC remains unaffected by any transitions of IC for till a duration of 40 seconds. The MIC is used as an input to the Gated Astable instead of IC. It is clear that this arrangement takes care of any transients which are of a duration less than 40 seconds, due to power failure.

This circuit puts restriction in the sense that the mode can not be switched to CLOCK from FREE unless and until it is ensured that the FREE mode was on for a minimum of 40 seconds. This is so because in such an event the command to switch to CLOCK mode will be treated as a transient and the Gated Astable will remain free-running whereas the D FF of the Mode Selector is manually cleared. The MCS start thus would no longer be inhibited and the Address Register will be cleared just after every positive edge of the MCS start; thus the synchronism between the Memory Locations and the Address Register will be lost.

This catastrophe is averted by using the $\overline{Q}$ output of the second monostable of Fig. 5.1, instead of Vcc to clear the Mode Selector FF when the CLOCK mode is chosen, as shown in Fig. 5.1.

To reduce the drain on the DC batteries we have to put the display off during the back up. This is ensured by simply supplying no back up power to the entire display Unit.

Special care has to be taken regarding the channel identification. Unless we are in a position to identify all the channels after the power comes back, the data preserved in the Memory has no meaning. One of the ways to ensure this would be to supply the Address Register with the back up power. But since these are high power TTLs (3 EC 79 Os) the demand on the back up unit will be extravagant.

Another method of preserving channel identification would be to embed the information in the Memory itself. Because the Memory is circulating the identification of all channels is possible if we can identify any particular channel. As there is a fixed relation between the channel number and the Channel Clock, the total

number of Memory Locations can not be altered and no extra location can be added for the purpose of identification. Hence we have to store the information of channel tracking in one of the regular channels itself. We choose the 256th channel for this purpose.

As we are following BCD code, the bits of no digit of any channel can be 1111. Making use of this fact we store 1111 in every digit of the channel 256. Though the Address Register is switched off during the back up, still we can identify all the channels once the power comes back as 256th channel can be always traced because of the bits stored in it.

The circuit of 5.2 describes the arrangement to realise the above method. As only 256 channel has to be loaded with the 1111 bits some special cares have to be taken. The outputs of 256 channel should by-pass the BCD adder. The 1111 bits should be basically recirculated once they occur at the output, for that particular digit. Hence the Erase operation must precede the loading of 1111 bits into 256 channel, as if at all, there is any channel with 1111 bits in any of its digits, these bits will be always recirculated because of the above mechanism.

The operation of loading 1111 bits into the six digits of 256 channel is referred to as "Initialise" operation.

A switch is provided on the panel to follow the sequence of operations: Erase, Initialise and Operate. It can be also verified that the circuit of Fig. 5.2 is safe against any contact bounces caused by the manual switch.

The total saving in the back up current requirements due to the above method of identification of the channels is of the order of 300 mA.

As we are automatically switching the instrument to FREE mode and as arrangement for channel identification has also been incorporated during the back up the data will be preserved during any power failure. To take care of the transient that might be associated with the power come back, it is advisable to switch the instrument to FREE mode, once the user knows regarding the power failure. Suggestions for eleminating this necessiti are made in Chapter 6.

CHAPTER VI

SUGGESTIONS FOR IMPROVING THE PERFORMANCE OF THE MCS

In this chapter we suggest some methods to improve the overall performance of the Multi - channel Scaler.

6.1 The Memory

This is the costliest component that has been used in the entire unit. An optimum choice of this can result in overall cost reduction and compactness.

TMS 3401 the dynamic memory chosen at the time of starting this project was the highest bit/chip memory available at that time. Today chips with still higher bits are available in the market and their use would result in the reduction of total chip count. The main factor to be considered is that for 256 channels we need four 1536 bit serial shift registers. As the bits per chip are as a rule powers of 2, 512 bits/chip were the maximum possible bits that could have been used for 256 channels. It is clear that in case the channel number is expanded to 512 chips with higher bits (as 1024 bits/chip)

could be used.

The maximum memory advance rate required in the system is 300 KHz. The TMS 3401 offers a maximum of 5 MHz advance rate. A chip with lower high frequency limit could be used if available at a lesser cost.

The minimum clock rate specified for the system is 2.5 KHz. At this rate the TMS 3401 places a stringent restriction on the Gated Astable design. These restriction can be removed by using a chip having a lower frequency range.

6.2 Low Power TTL

We have opted for TTLs in hardware realisation because they offer the highest performance/cost ratio. The MCS system as such is quite slow. Low power TTLs will be an optimum choice as they will considerably reduce the total power requirements. This factor is very important when we consider the back up supply. Atleast those units of the Control Logic that are supplied with back up power must incorporate the low power TTLs. (We could not use these low power TTLs because of their lack of availability.)

6.3 Channel Overflow

In the present unit we have not made any arrangements to counter a situation where a channel count exceeds 999999. In such an event the channel count will restart from zero after the overflow. Figure 6.1 suggests a shceme that will stop the Data intake whenever there is any channel overflow. Visual indication can also be incorporated to indicate the channel overflow if any, as shown in the figure.

6.4 Back up ON Indicator

In the present system there is no way of knowing whether the power failure safeguard scheme is working or not. Figure 6.2 suggests a scheme that will give an indication if the back up system is working during a power failure. We have exploited the fact that only during the power failure IC and $\overline{IC}$ will both be at Logical 1. MIC = 1 ensures that the memory circulation is maintained. The lamp in the figure indicates the same.

6.5 Power Failure Relay

We have mentioned in Chapter 5 that the user should manually switch the MCS to FREE mode once he knows

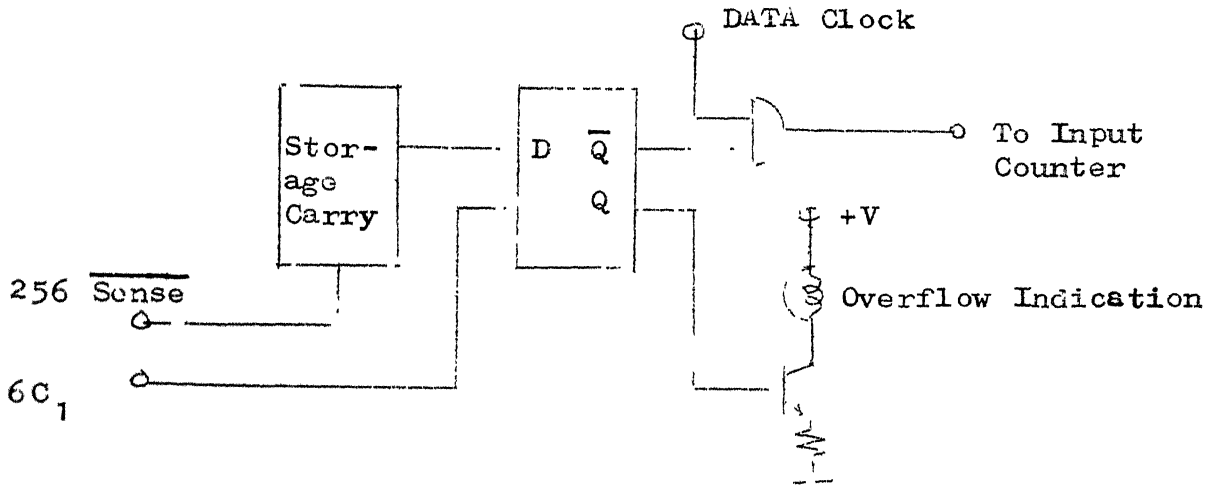

Fig. 6.1 CHANNEL OVERFLOW

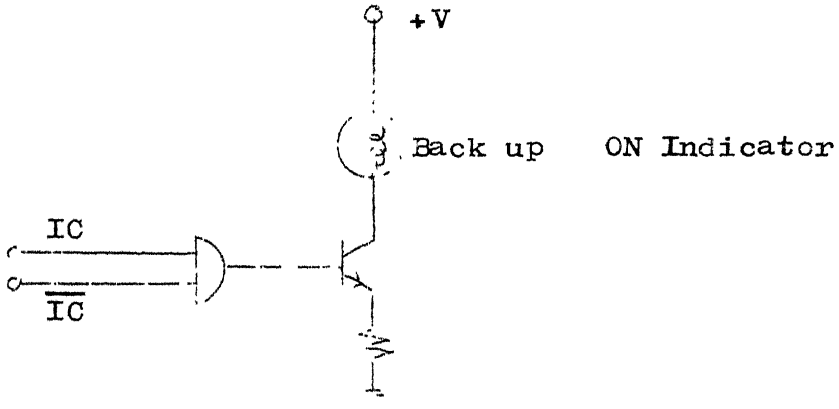

Fig. 6.2 BACK UP ON INDICATOR

that the power has failed. A relay can be incorporated in the system to automatically take it to the FREE mode whenever power fails. Special care has to be taken to ensure that the relay contacts do not switch the instrument back to CLOCK mode as soon as the power comes back. It is obvious that this relay which elemenate the need for the user to be vigilant in case of a power failure should be energized from the main power line. Suitable Normally ON and Normally OFF contacts could be used for this purpose.